


Quanta Project Name: XM1

Dell Project Name: Nike

A00(QT) Stage

BOARD REV : E

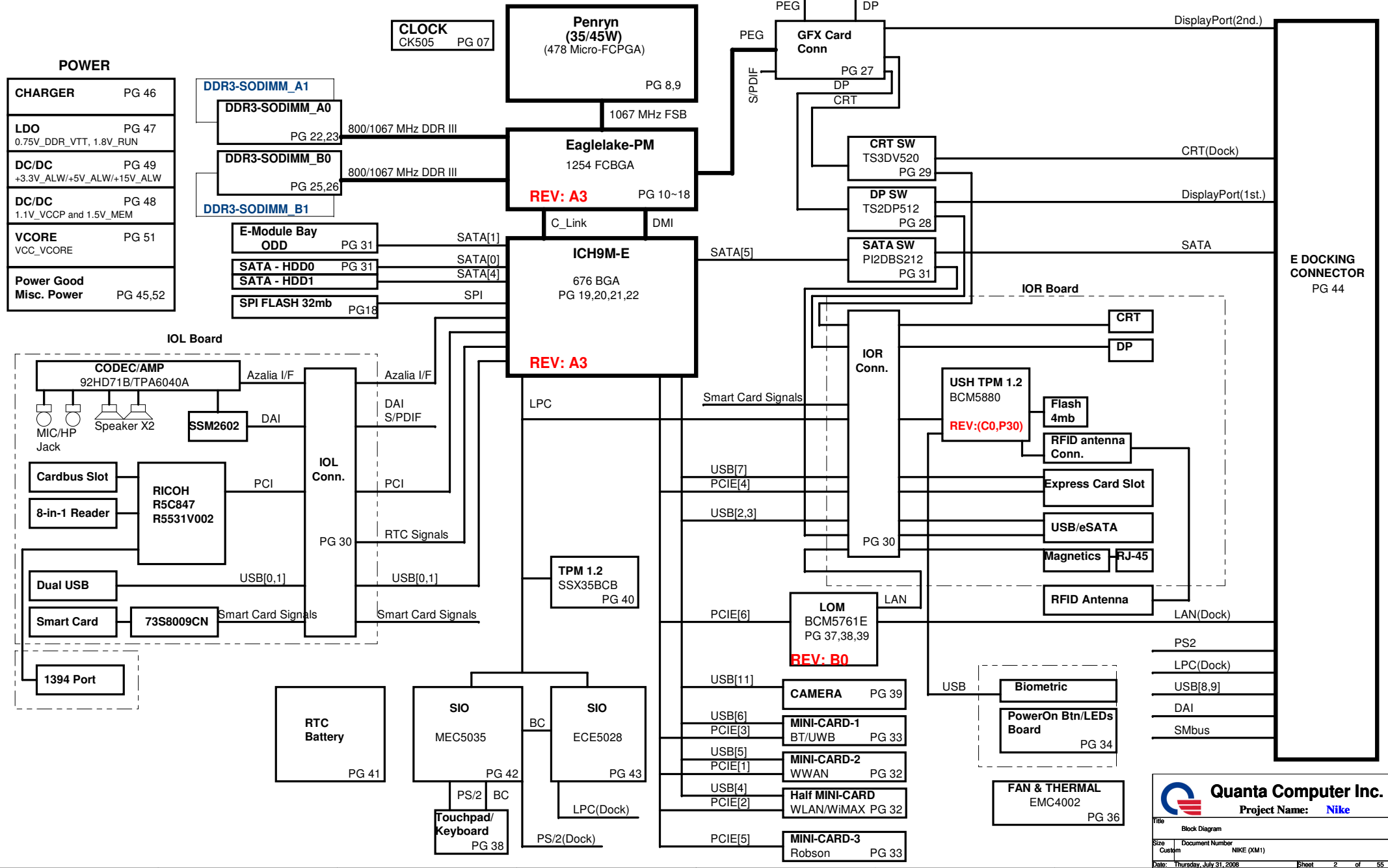
2008-07-25

		Quanta Computer Inc.	
		Project Name: Nike	
Title: Cover Page			
Size: Custom	Document Number: NIKE (XM1)		Rev: E
Date: Thursday, July 31, 2008		Sheet: 1 of 55	



System Block Diagram of Nike

PWA XXX, PWB XXX,
SCHEM XXX.
Board Ver : E
Date:20080716



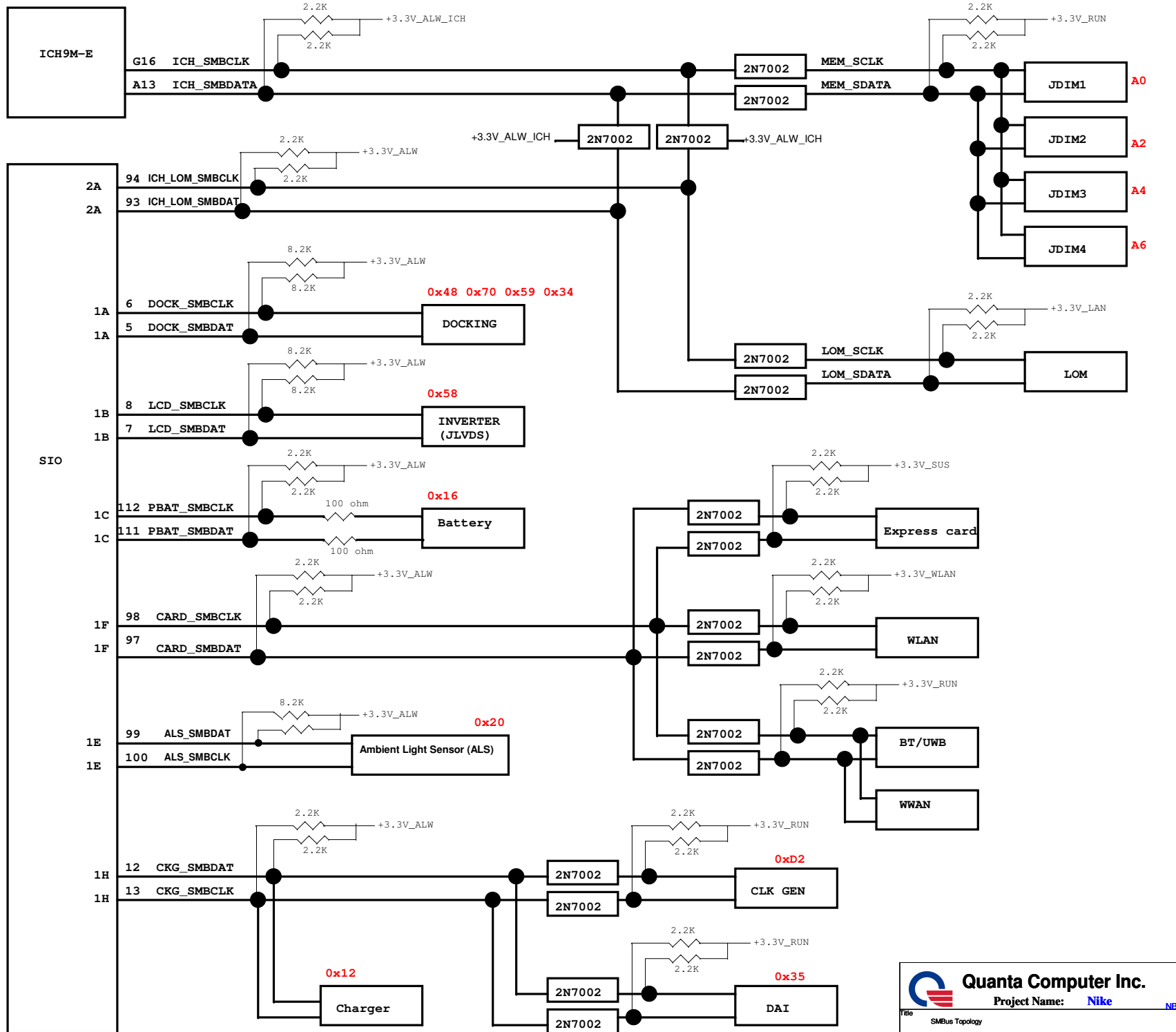
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07	Clock Generator
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27	GFX CARD CONN.
28	DisplayPort SWITCH
29	CRT SWITCH
30	IOR and IOL connector.
31	SATA(HDD_ODD) eSATA SWITCH
32	MINI Card
33	MINI Card
34	TP PWR BUTTON
35	CCD SNIFFER LED.
36	THERMAL EMC4002
37~39	BCM5761E_LOM
40	SSX35BCB (TPM for China)
41	RTC BATTERY
42	SIO_MEC5035
43	SIO-ECE5028
44	E-DOCKING CONNECTOR.
45	System Power Good.
46	Battery Charger.
47	0.75V_DDR_VTT, 1.8V_RUN
48	1.1V_VCCP and 1.5V_MEM
49	5V_ALW, 3V_ALW
50	DCIN, Battery Connector
51	CPU_VCORE (ADP3207A)
52	Power Misc
53	Screw hole

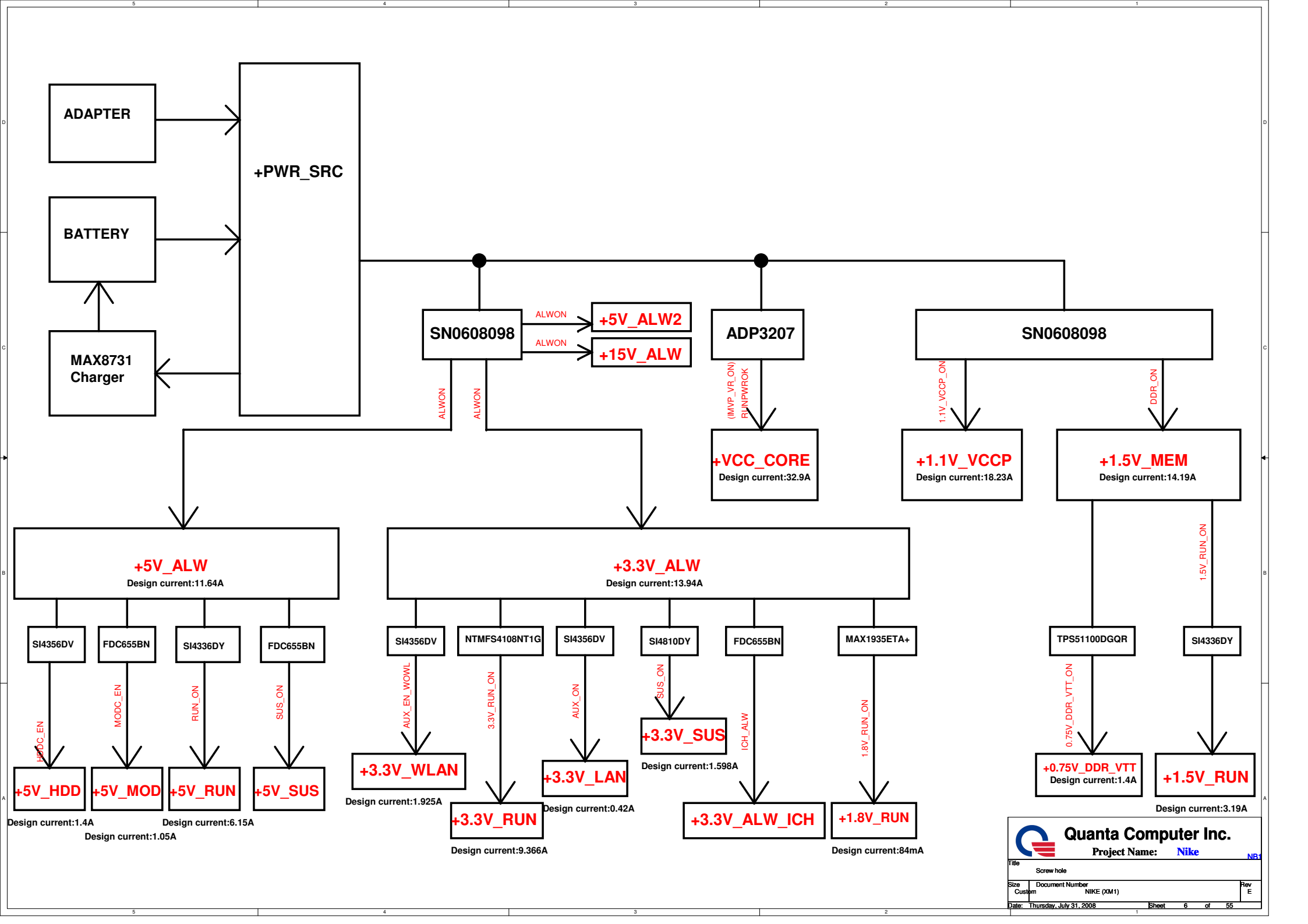
Signal State	SLP S3#	SLP S4#	SLP S5#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

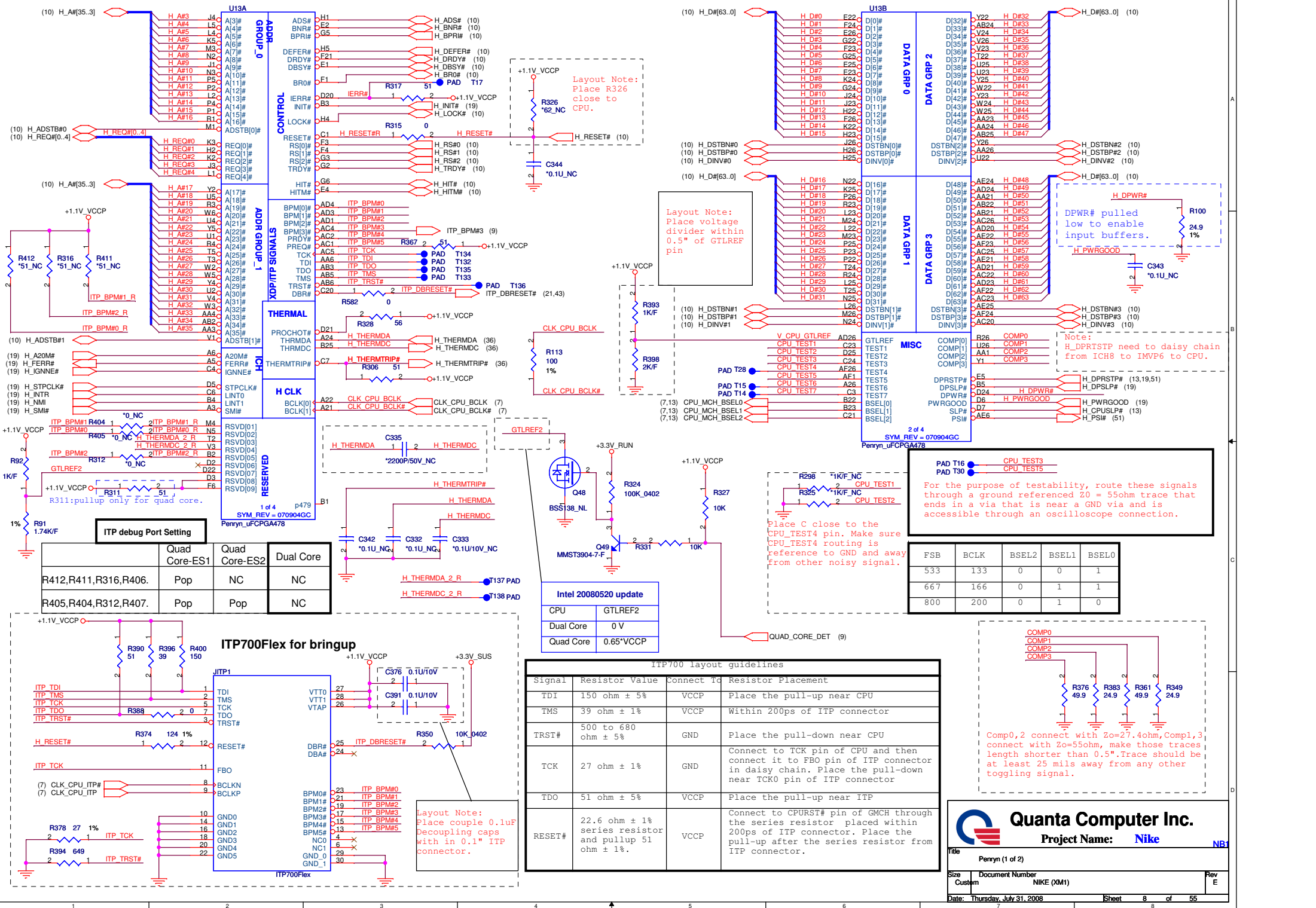
Power Plane State	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +1.1V_VCCP +VCC_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

ICH9M-E	USB PORT#	DESTINATION
	0	Left Top
	1	Left Bot
	2	Right Top
	3	Right Bot
	4	WLAN
	5	WWAN
	6	WPAN
	7	Express card
	8	DOCKING
	9	DOCKING
	10	USH
	11	Camera

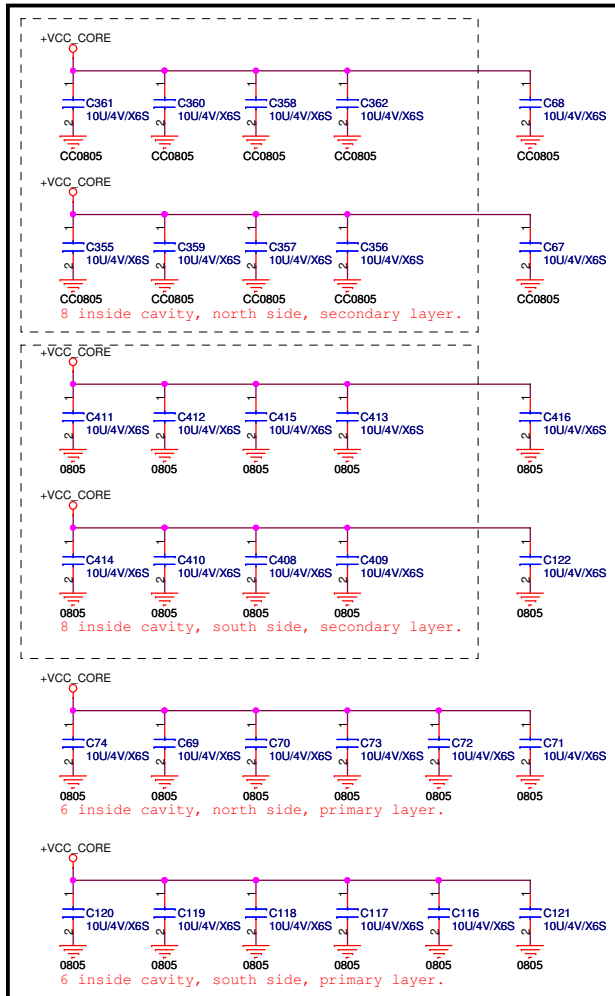
ICH9M-E	PCI EXPRESS	DESTINATION
	Lane 1	WWAN
	Lane 2	WLAN
	Lane 3	BT/UWB
	Lane 4	Express Card
	Lane 5	Robson
	Lane 6	Giga Bit LOM



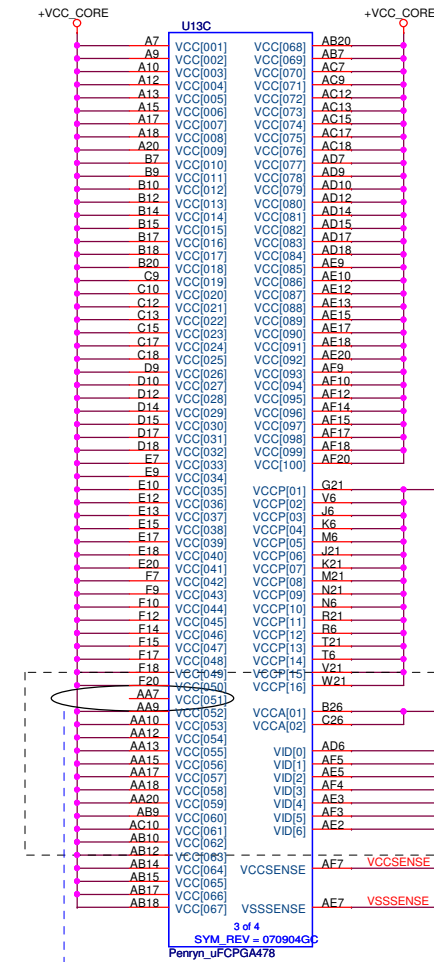




All use 22U 10V(+20%,X5R,1210)Pb-Free.



Layout out:
Place these inside socket cavity on North side secondary.



Pins AA7, AA8, AC8, D8 need to be NC for QC

Pins AA7, AA8, AC8, D8 need to be NC for QC

20080520 Intel update:

Penryn QC GTLREF_CONTROL pin.

CPU	Pin F8
Dual Core	GND
Quad Core	Internal pull 50 ohm to VCCP

+1.1V_VCCP

+C396

270U

2

+20%

7343

12m

(8) QUAD_CORE_DET

+1.5V_RUN

C341

0.01U/25V

C399

10U/4V

Layout Note:

Place C105 near PIN

B26.

+VCC_CORE

R172

100F

VCCSENSE

VSSSENSE

R171

100F

Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

(8) ITP_BPM#3

ITP_BPM#3

R407

0 NC

+1.1V_VCCP

R406

51 NC

See page8

ITP table

setting

Pins AA7, AA8, AC8, D8 need to be NC for QC

ITP BPM#3 R



Quanta Computer Inc.

Project Name: Nike

Title

Penryn (2 of 2)

Size

Document Number

NIKE (XMT)

Date:

Thursday, July 31, 2008

Sheet

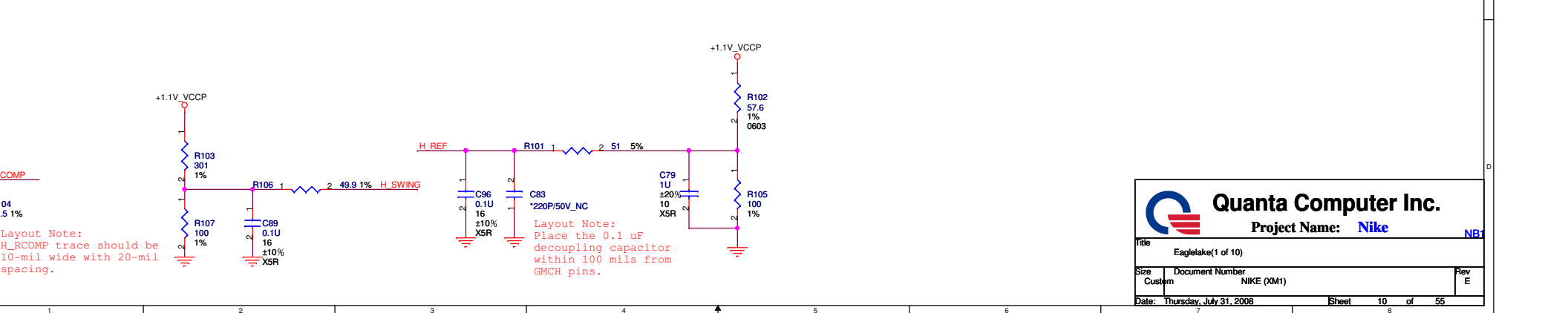
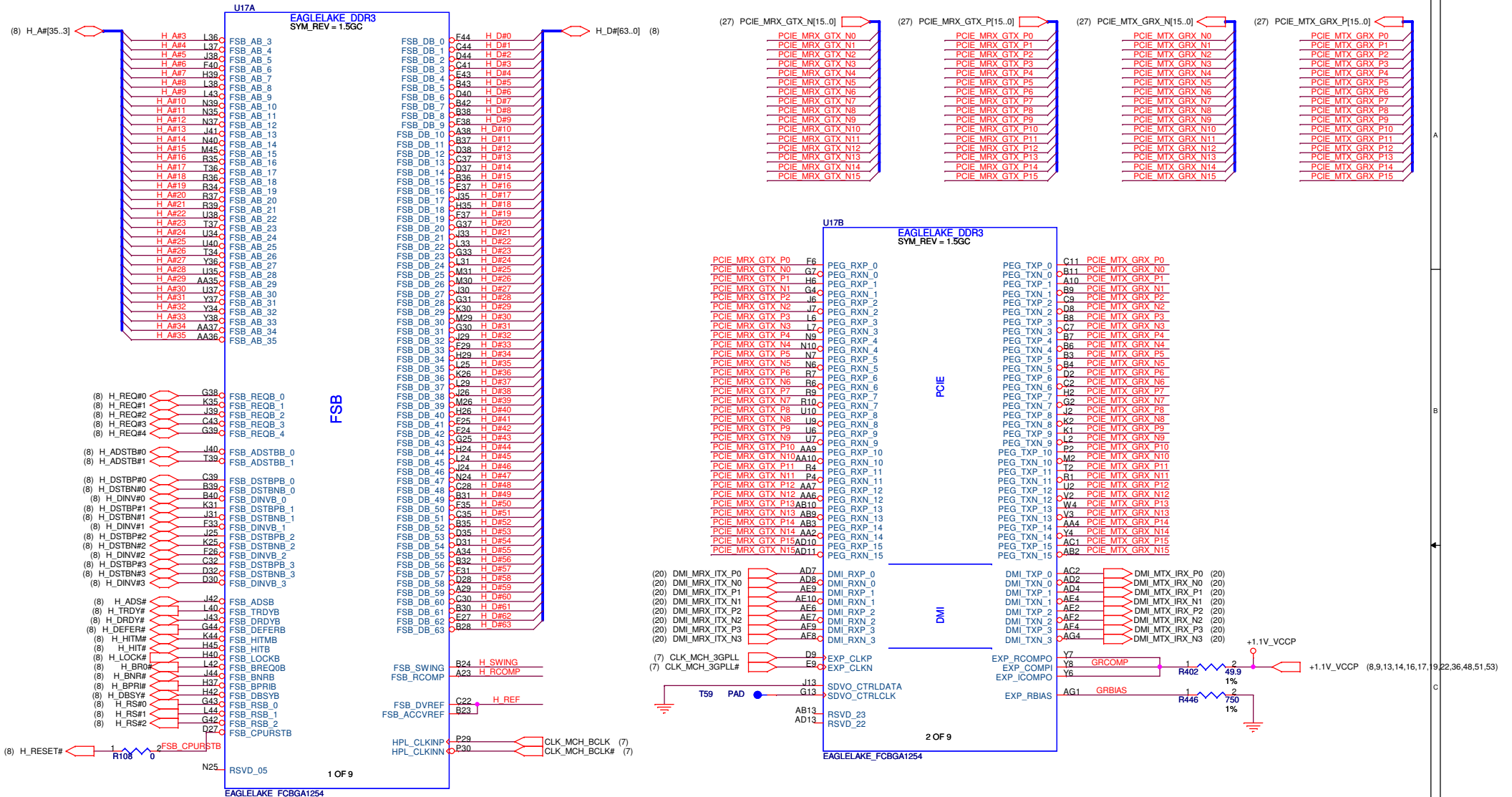
9


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55

Rev

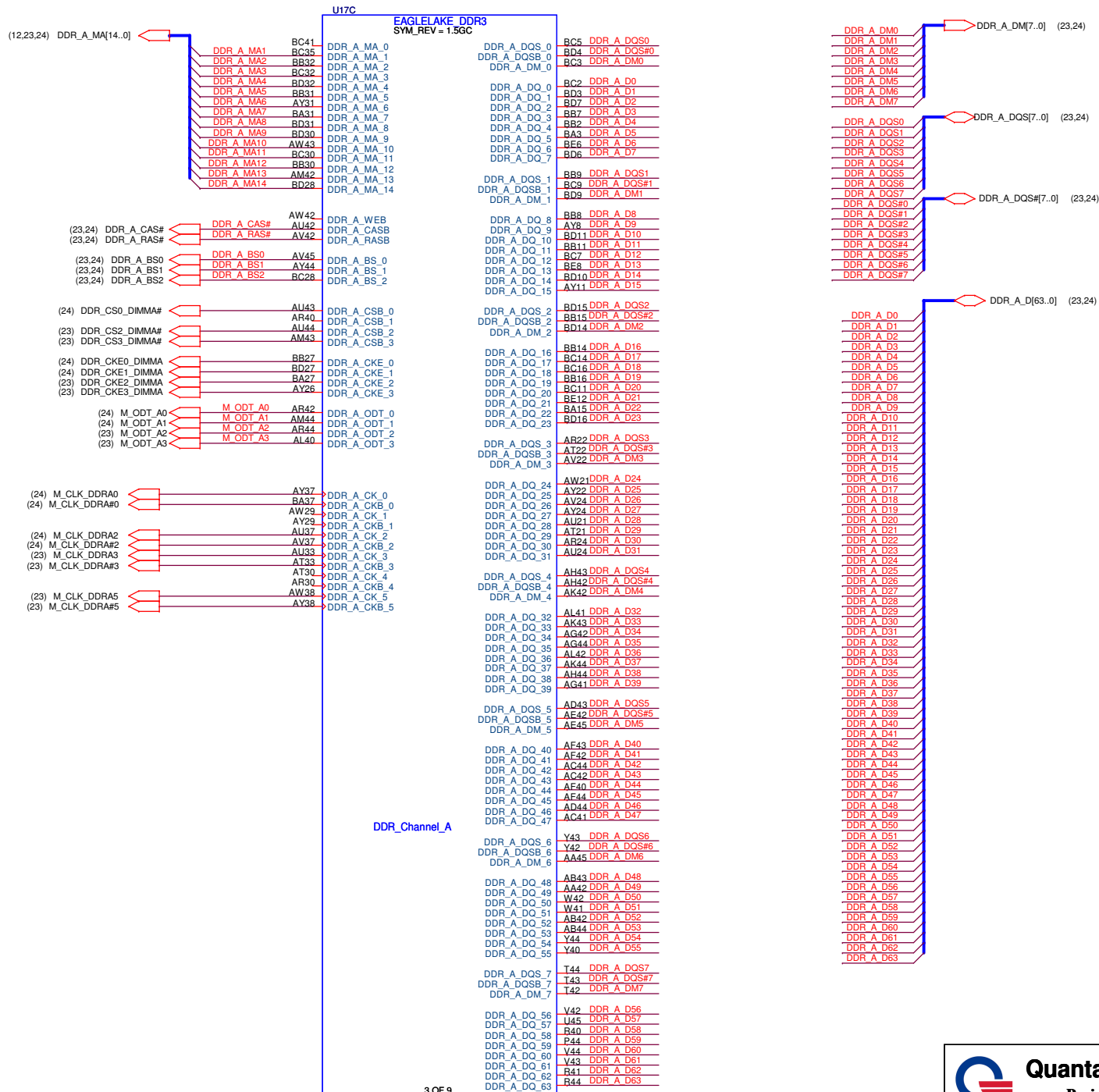
E






Quanta Computer Inc.
Project Name: **Nike**

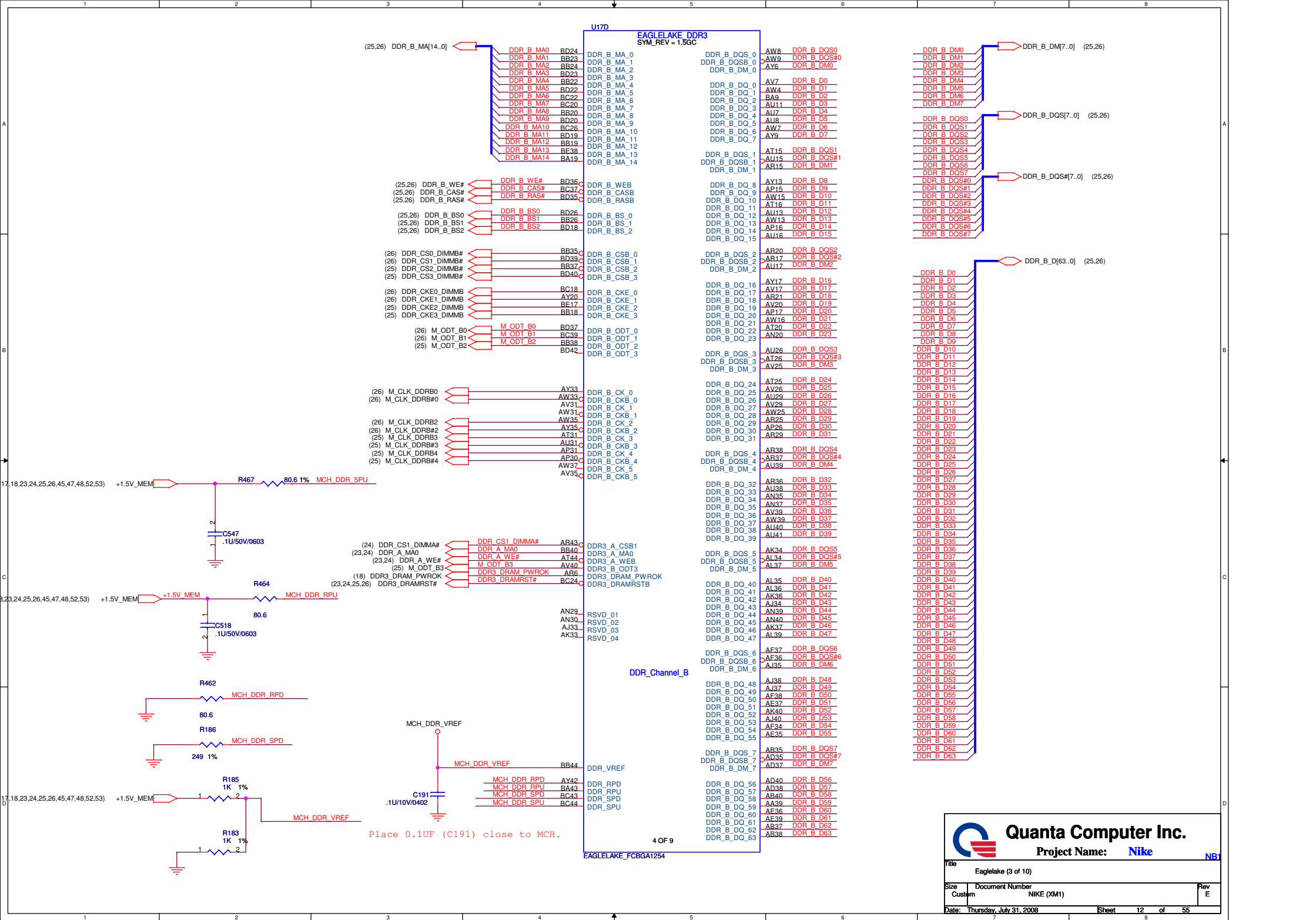
Title Eaglelake(1 of 10)		
Size Custom	Document Number NIKE (XMI)	Rev E
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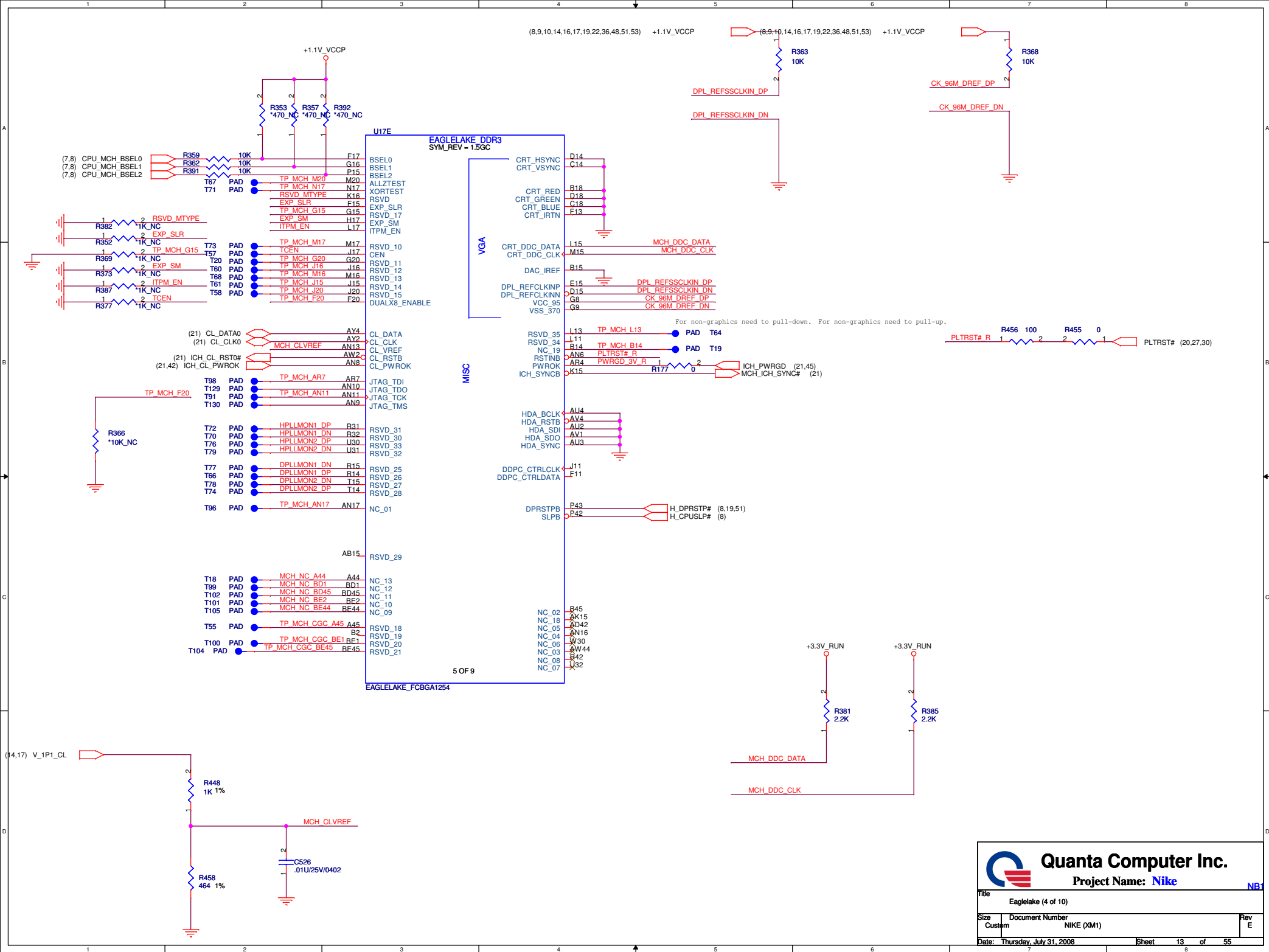


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EAGLELAKE_FCBGA1254

		
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EAGLELAKE_DDR3

GND


U171

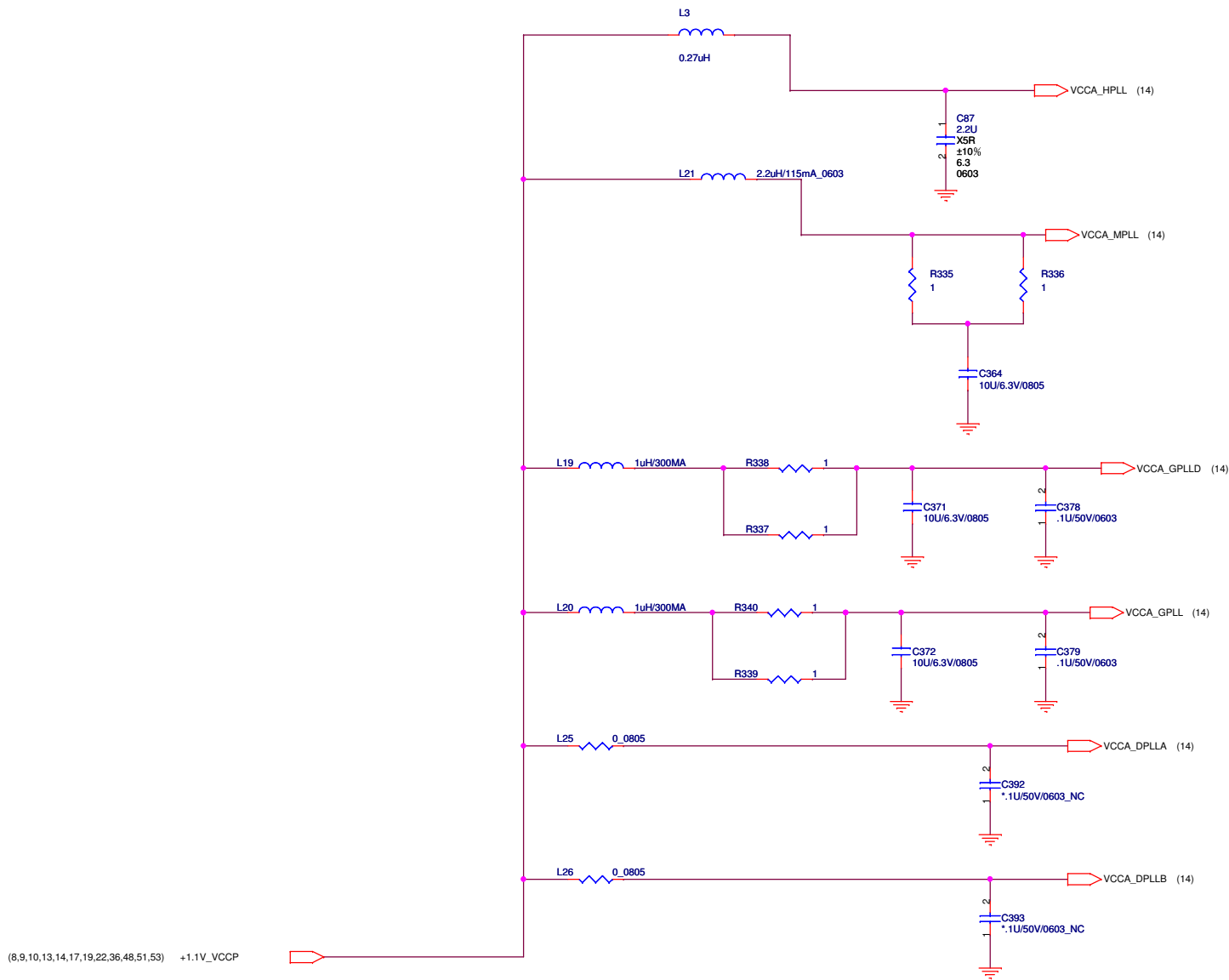
EAGLELAKE_DDR3
SYM_REV = 1.5GC

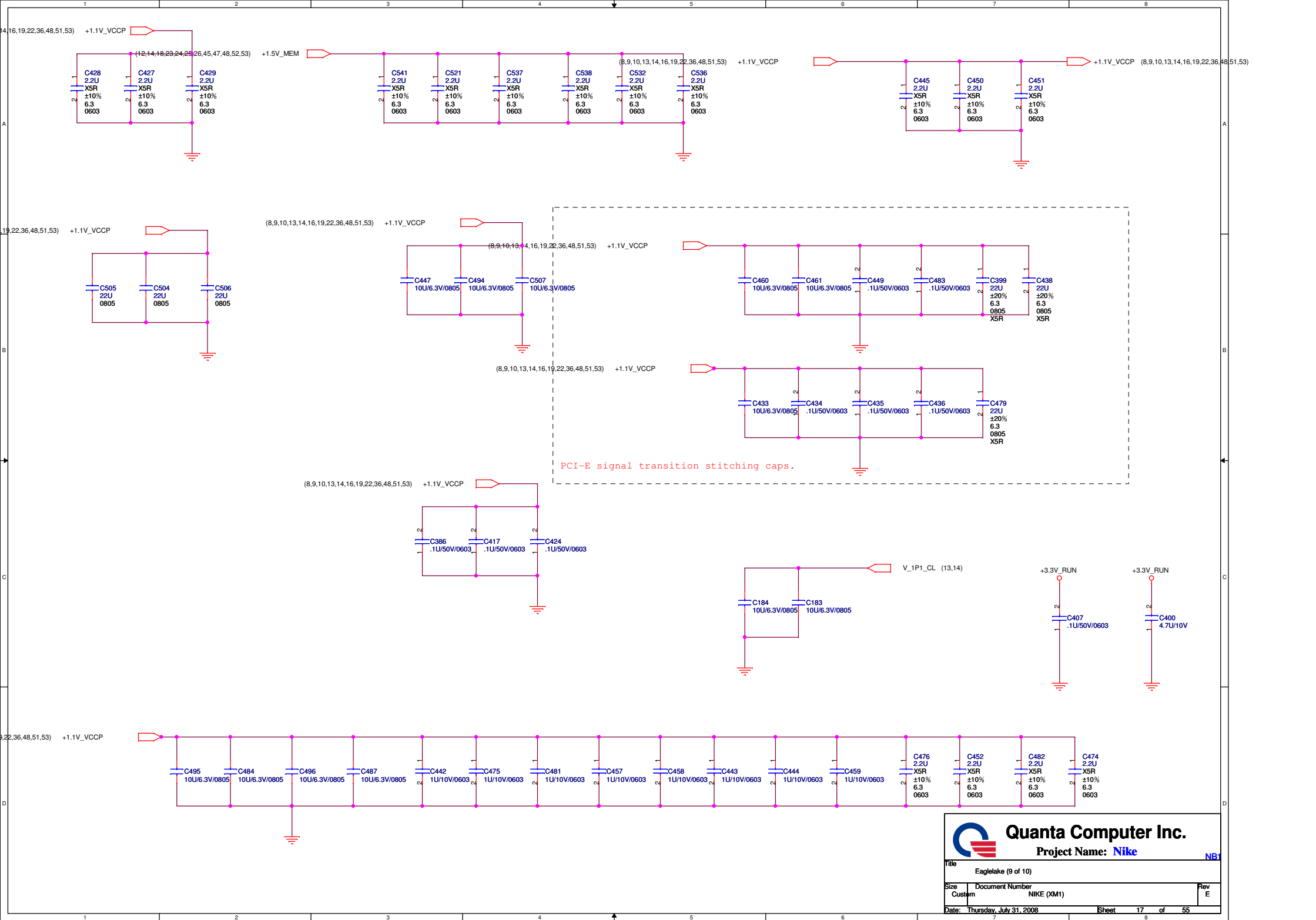
GND

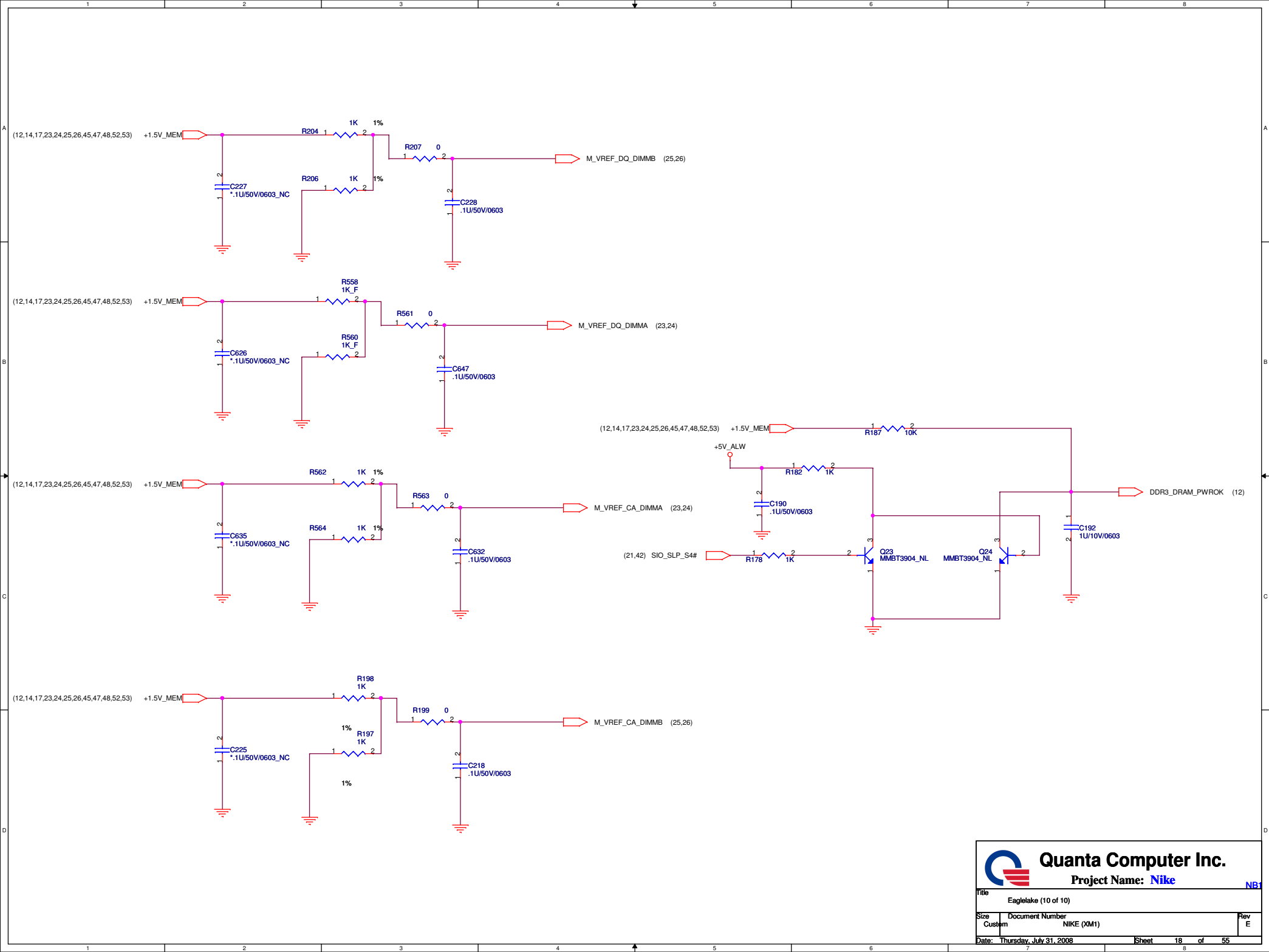
EAGLELAKE_FCBGA1254

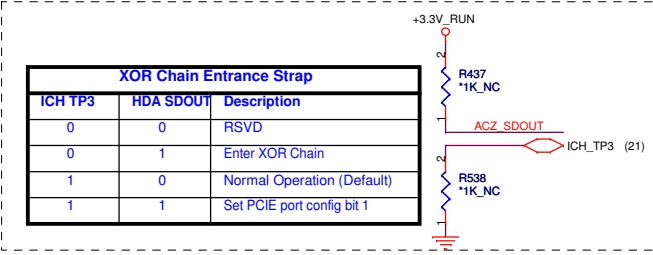
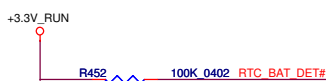
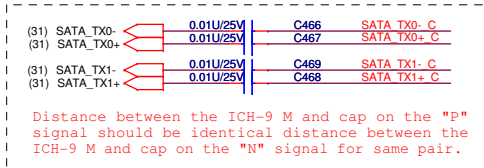
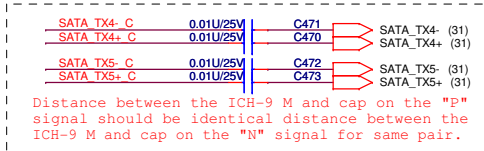
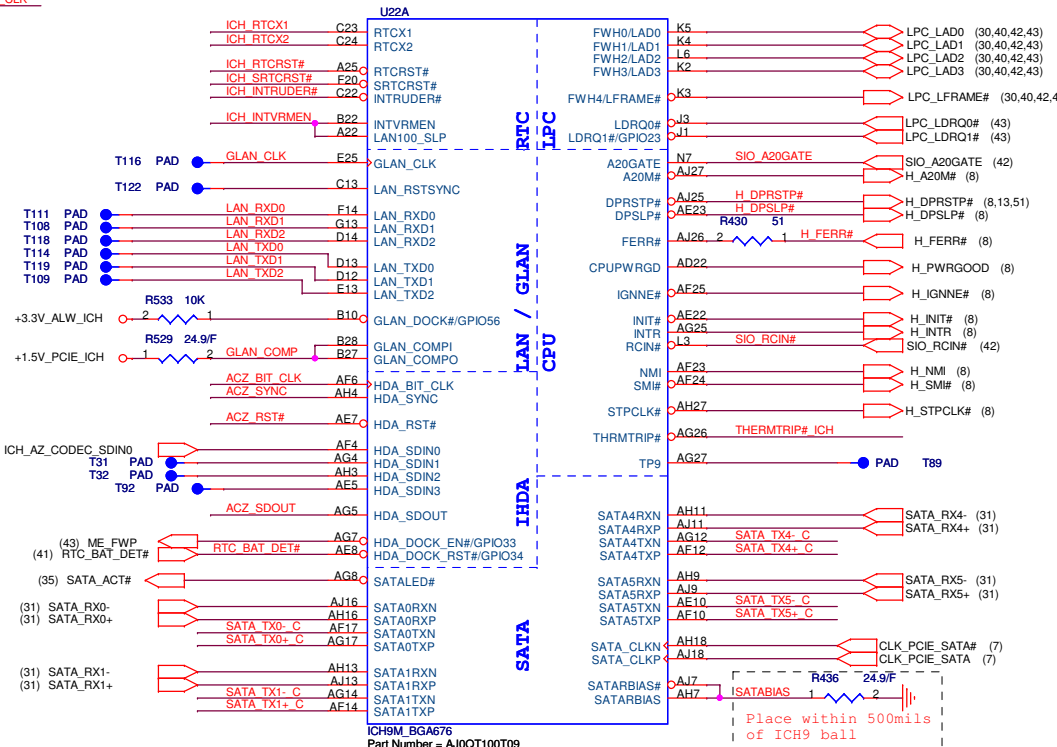
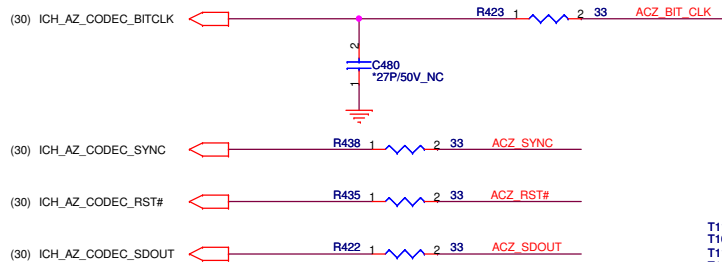
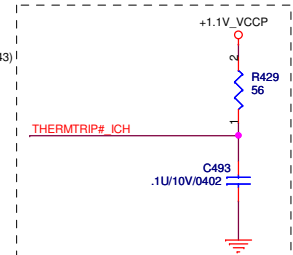
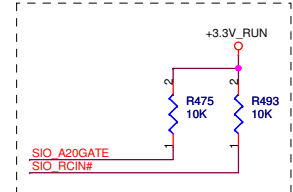
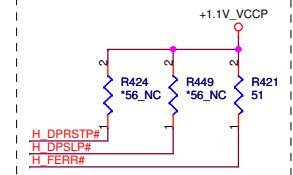
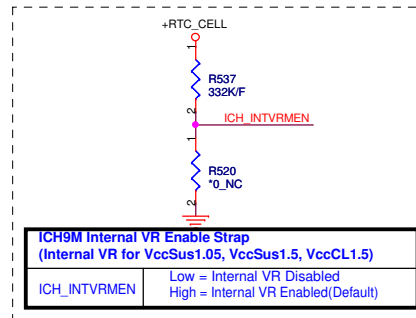
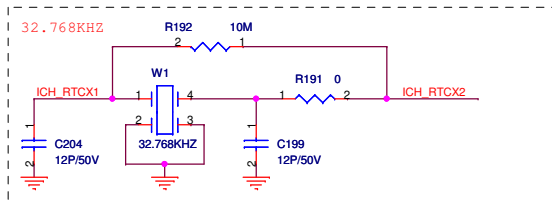
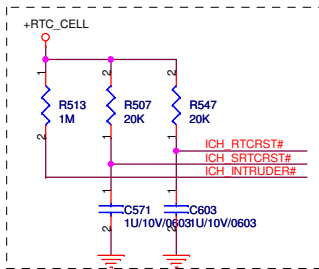
U17H
EAGLELAKE_FCBGA1254
SYM_REF = 1.5GC
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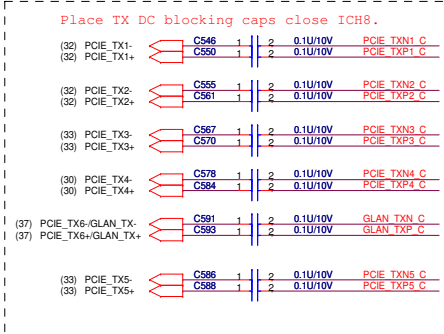
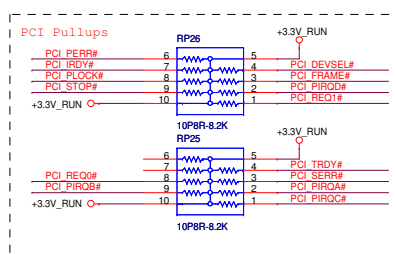




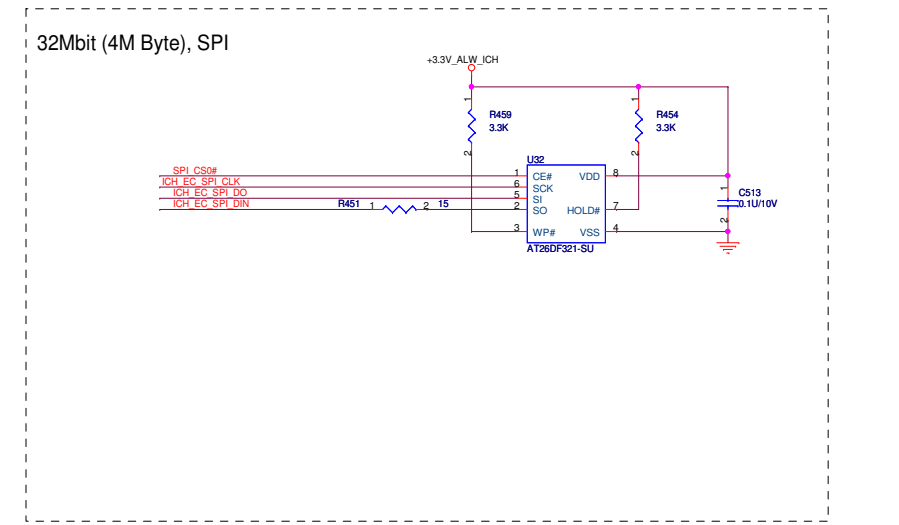
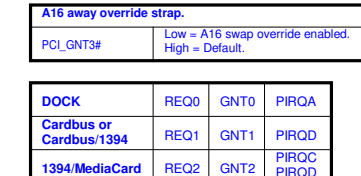
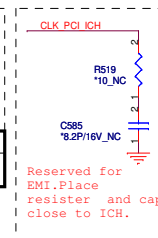
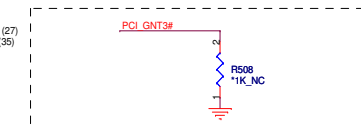
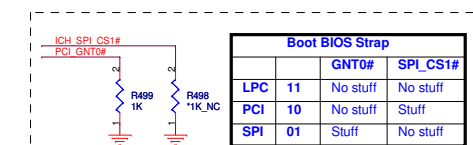
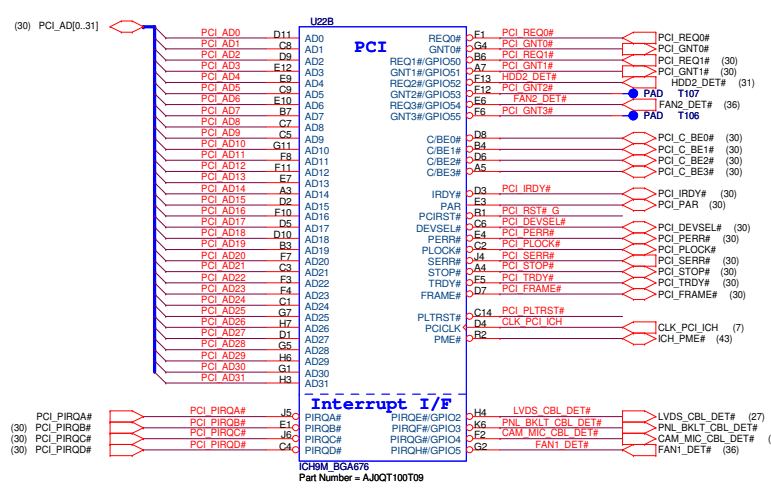
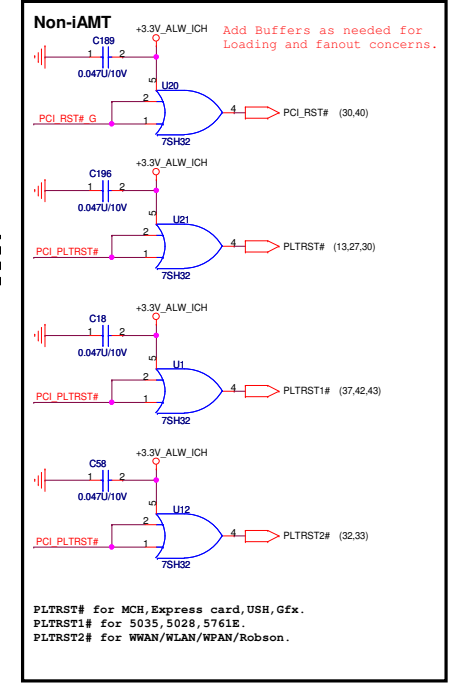
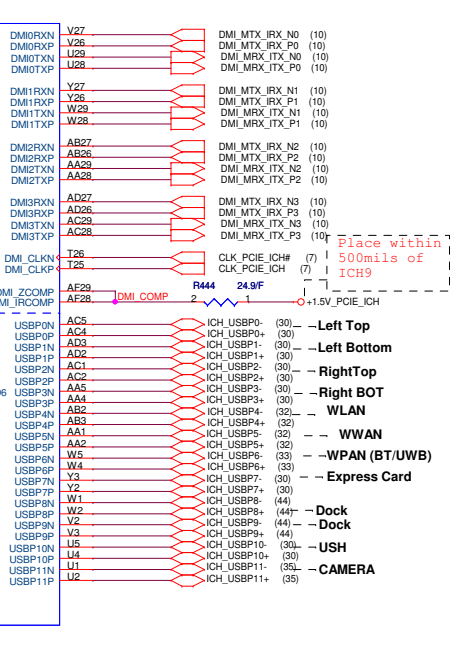
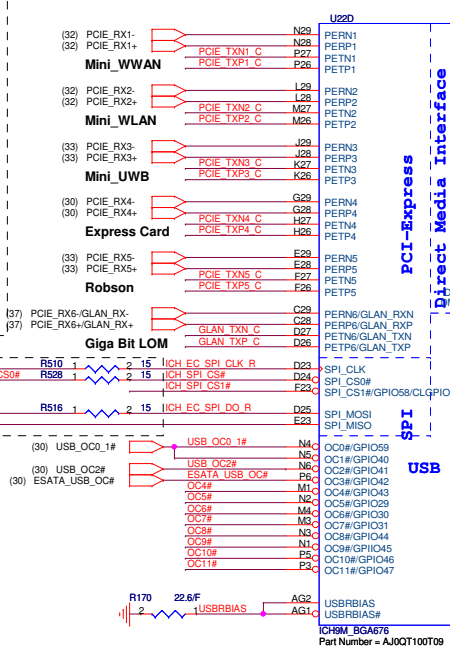


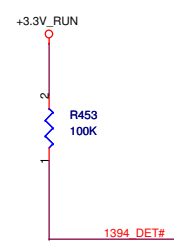
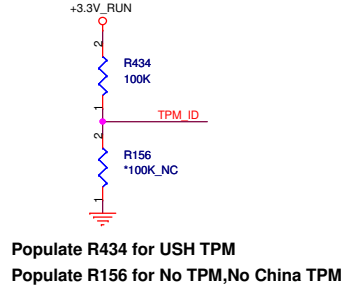
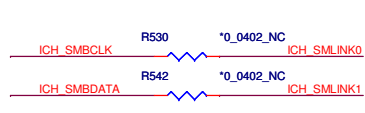
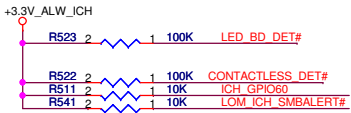
Quanta Computer Inc.
 Project Name: **Nike**

Title: ICH9M (1 of 4)		Rev E
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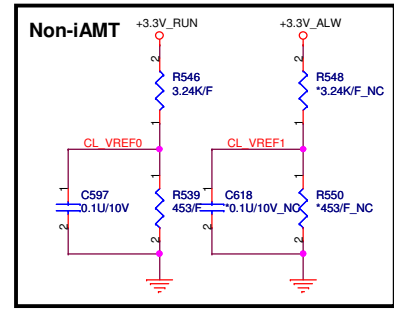
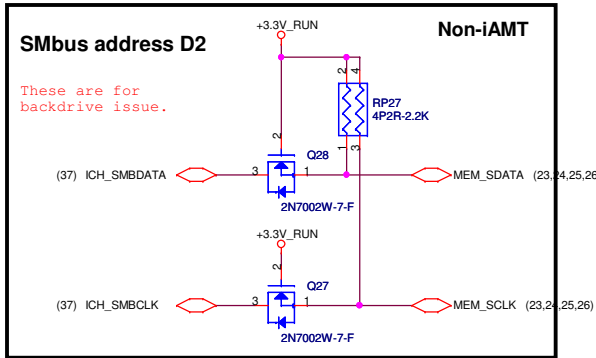
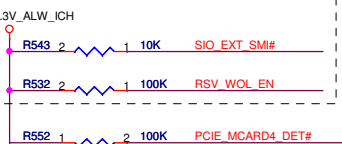
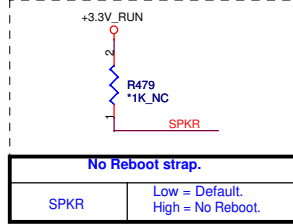
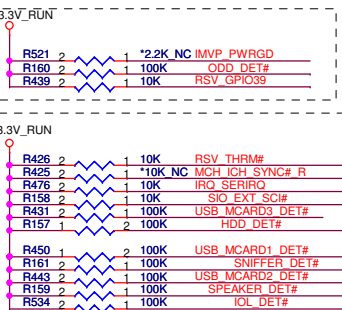
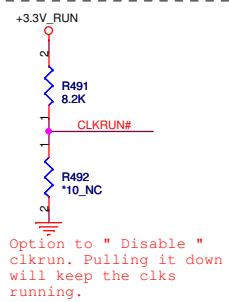
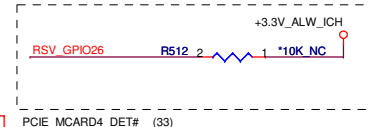
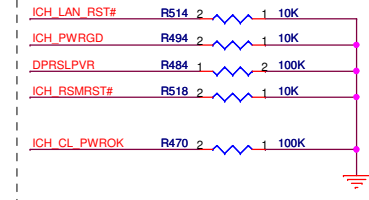
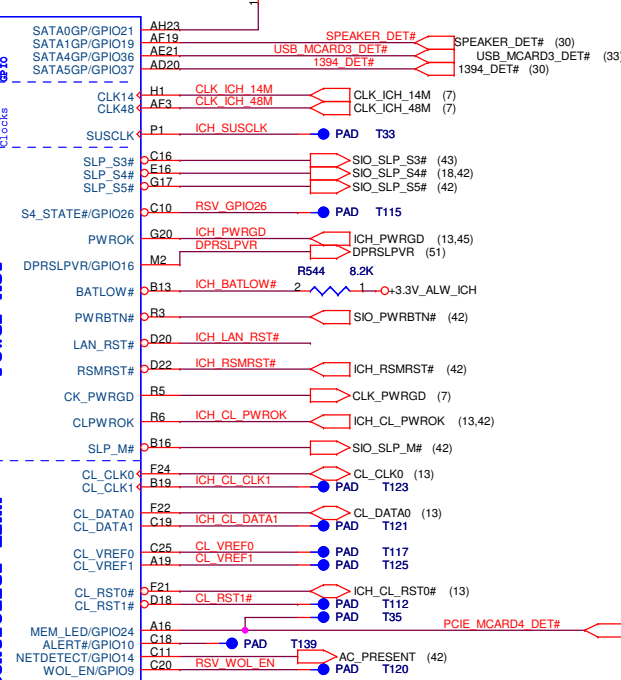
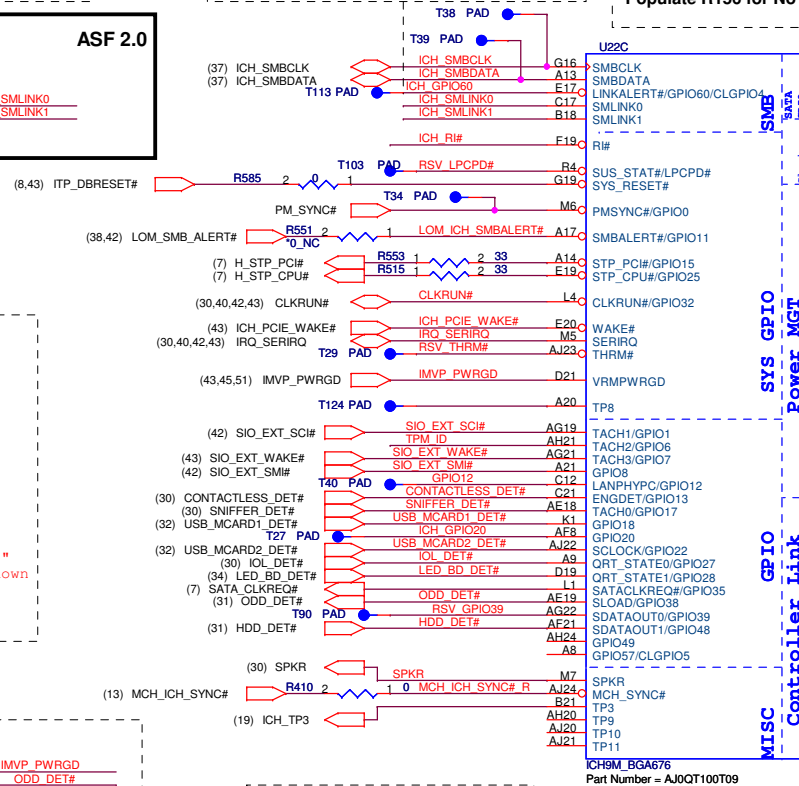
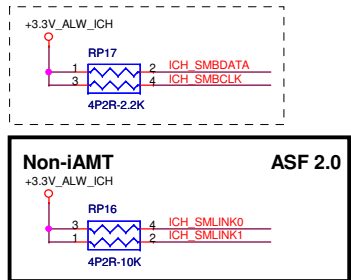
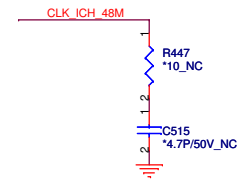


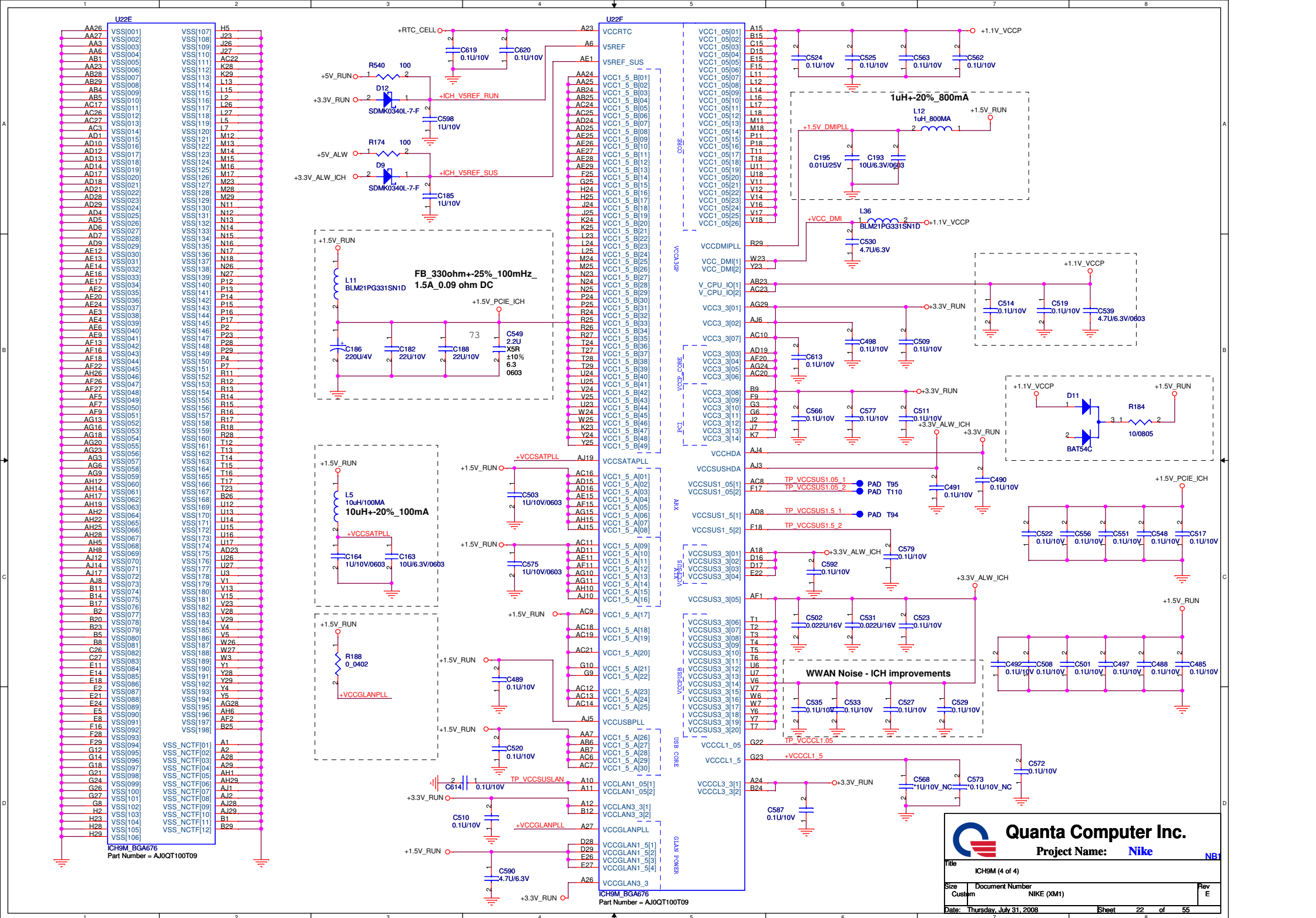
Layout Note:
Place R528, R506 within
500 mils from ICH.





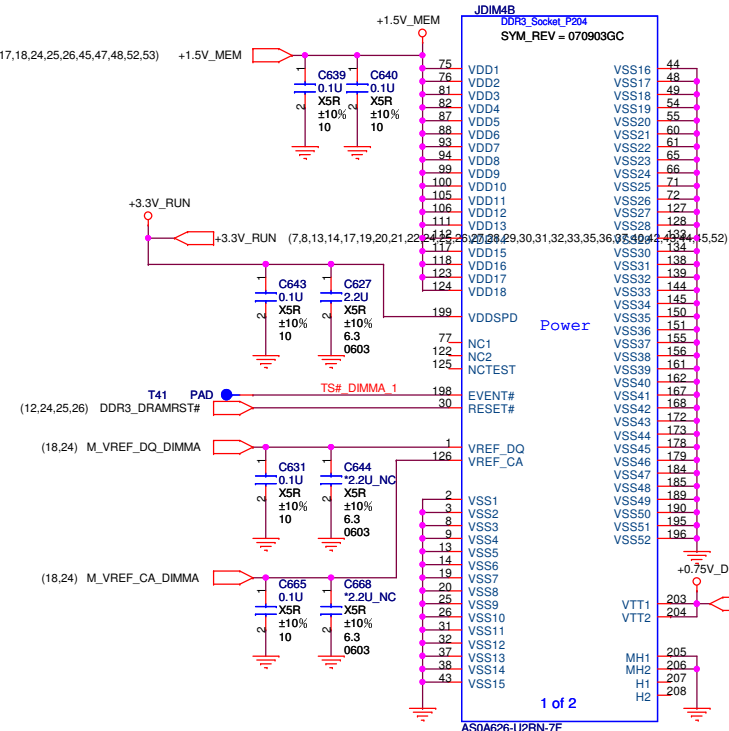
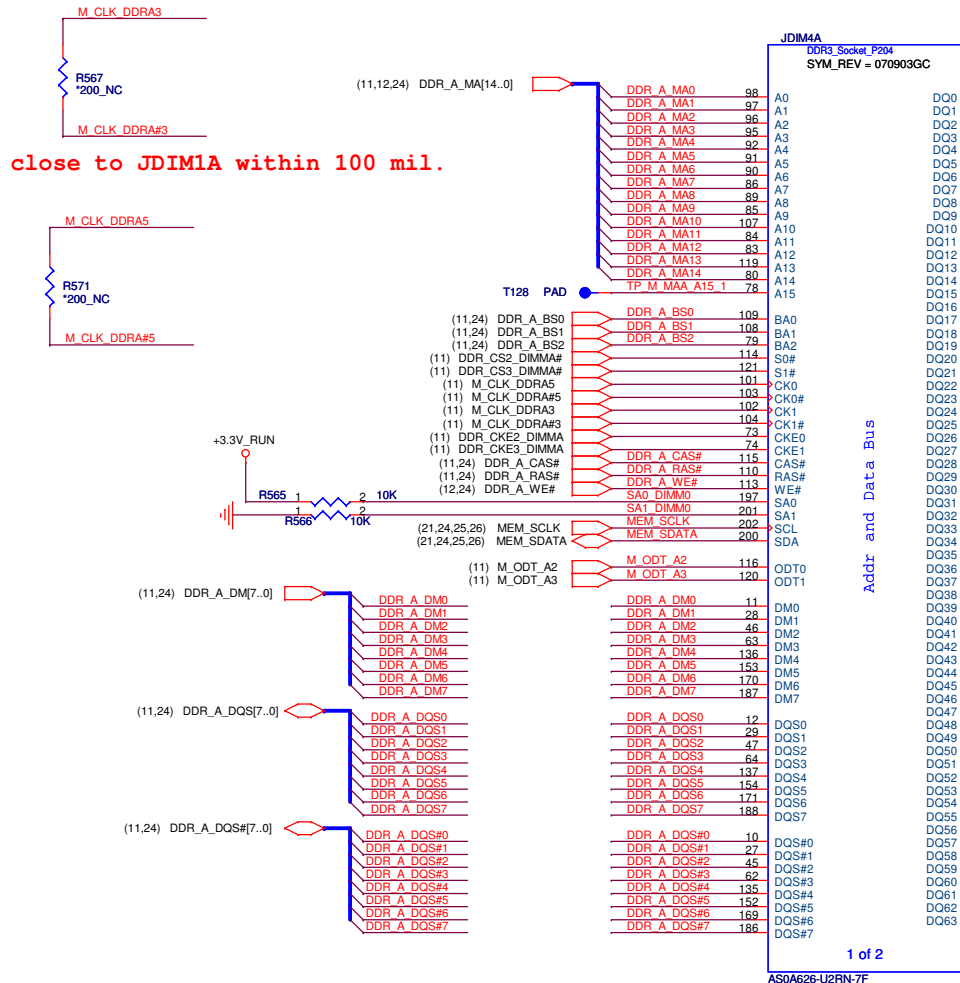
Place these close to ICH9.





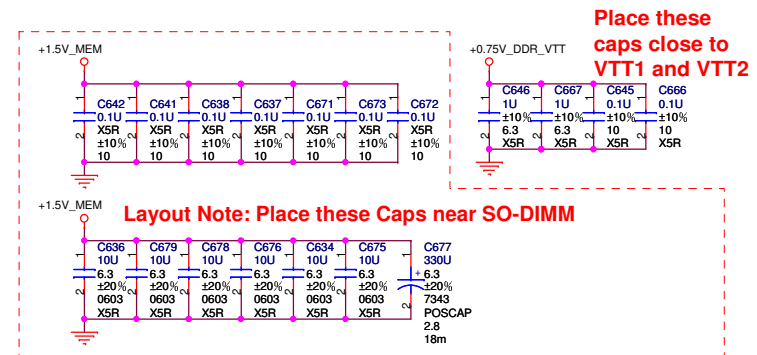
close to JDIM1A within 100 mil.

CHA_DIMM1_Bottom Layer



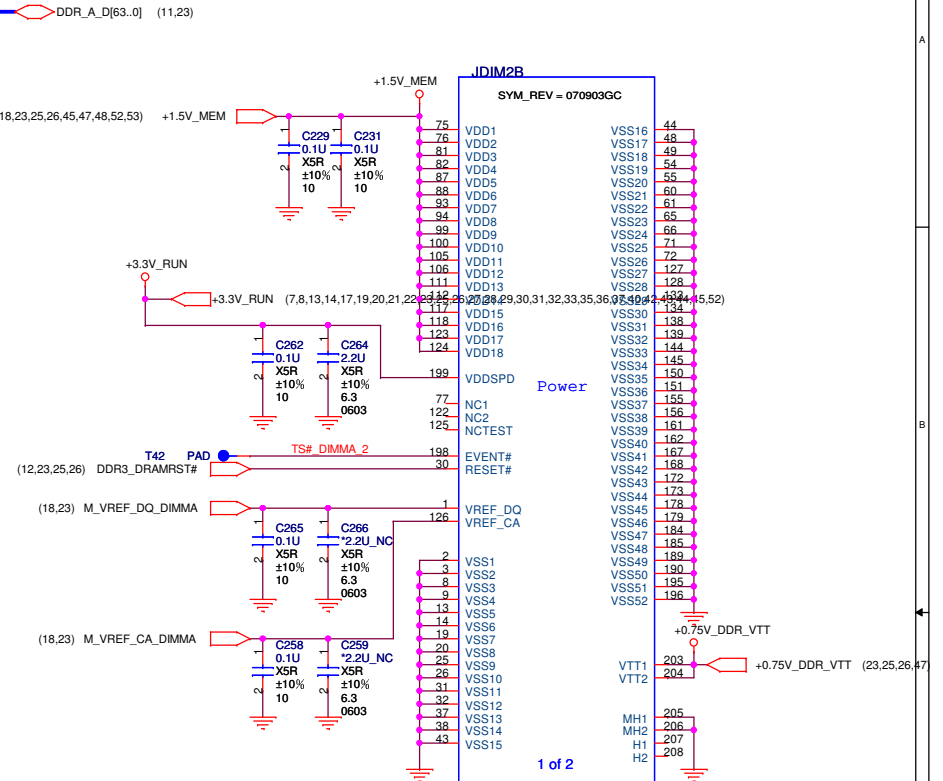
Select the Serial Presence Detect and Temp sensor base address.

	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	



Quanta Computer Inc.			
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CHA_DIMM0_TOP Layer



PCB Layout Diagrams for Capacitors near SO-DIMM

Top Left Diagram: Shows a row of capacitors (C272, C274, C270, C276, C268, C234) connected to +1.5V_MEM and ground. Each capacitor is 0.1U, X5R, ±10%, 10. The capacitors are labeled C272, C274, C270, C276, C268, C234, and C278.

Top Right Diagram: Shows a row of capacitors (C261, C233, C260) connected to +0.75V_DDR_VTT and ground. Each capacitor is 1U, X5R, ±10%, 10. The capacitors are labeled C261, C233, C260, and C272.

Layout Note: Place these Caps near SO-DIMM

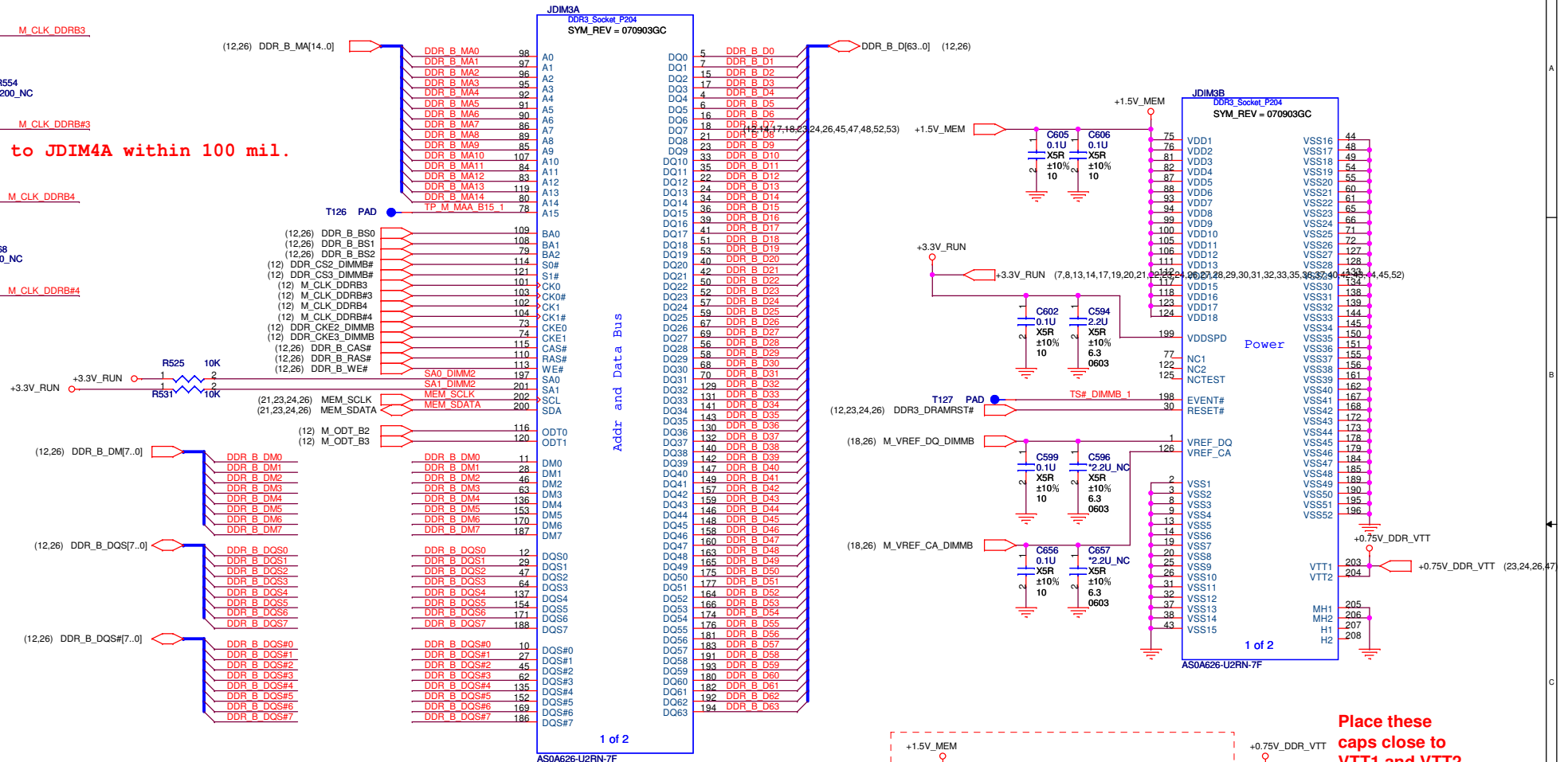
Bottom Diagram: Shows a row of capacitors (C273, C275, C277, C271, C269, C267) connected to +1.5V_MEM and ground. Each capacitor is 10U, X5R, ±20%, 0603. The capacitors are labeled C273, C275, C277, C271, C269, C267, and C263. A note indicates C263 is 330U, 6.3, ±20%, 0603, 7343, POSCAP, 2.8, 18m.

	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	

CHB_DIMM1_Bottom Layer

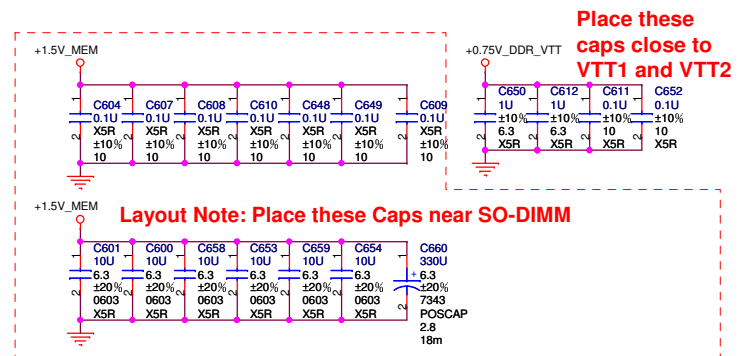
close to JDIM4A within 100 mil.

close to JDIM4A within 100 mil.



Select the Serial Presence Detect and Temp sensor base address.

	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	



Quanta Computer Inc.

Project Name: **Nike**

Title: **DDR3 Channel A0 (3 of 5)**

Size: **Custom**

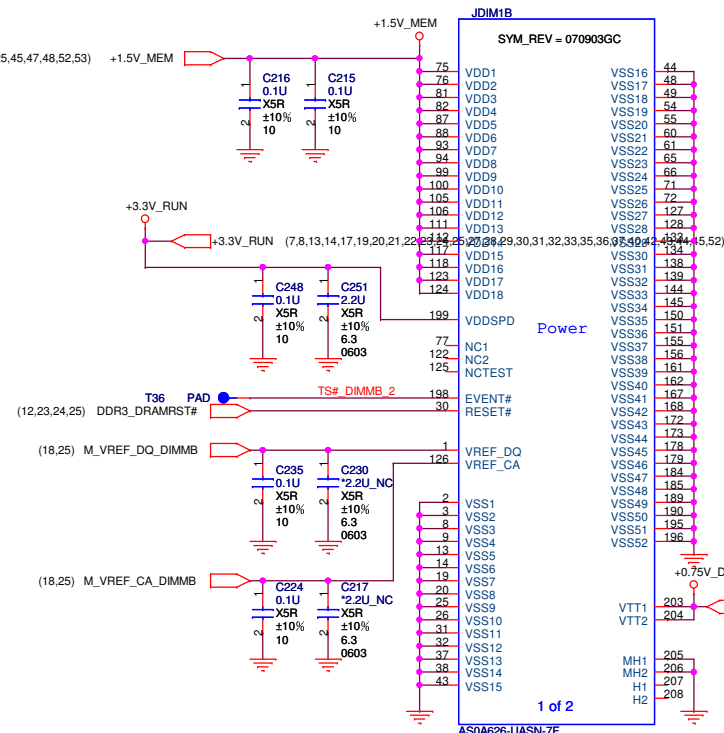
Document Number: **NIKE (XM1)**

Date: **Thursday, July 31, 2008**

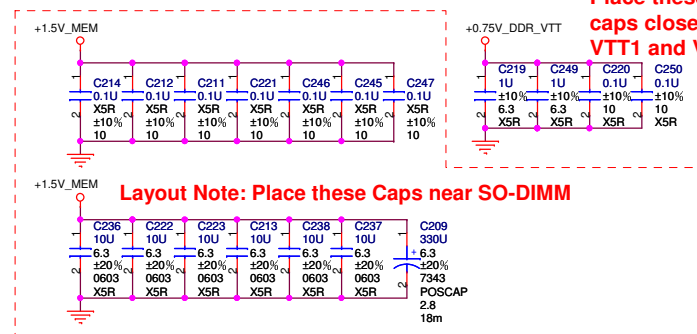
Rev: **E**

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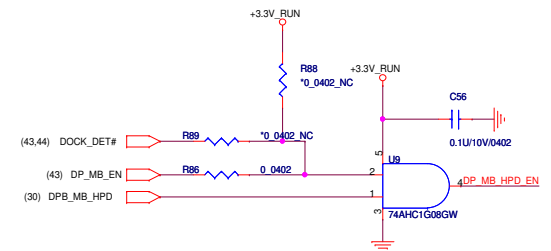
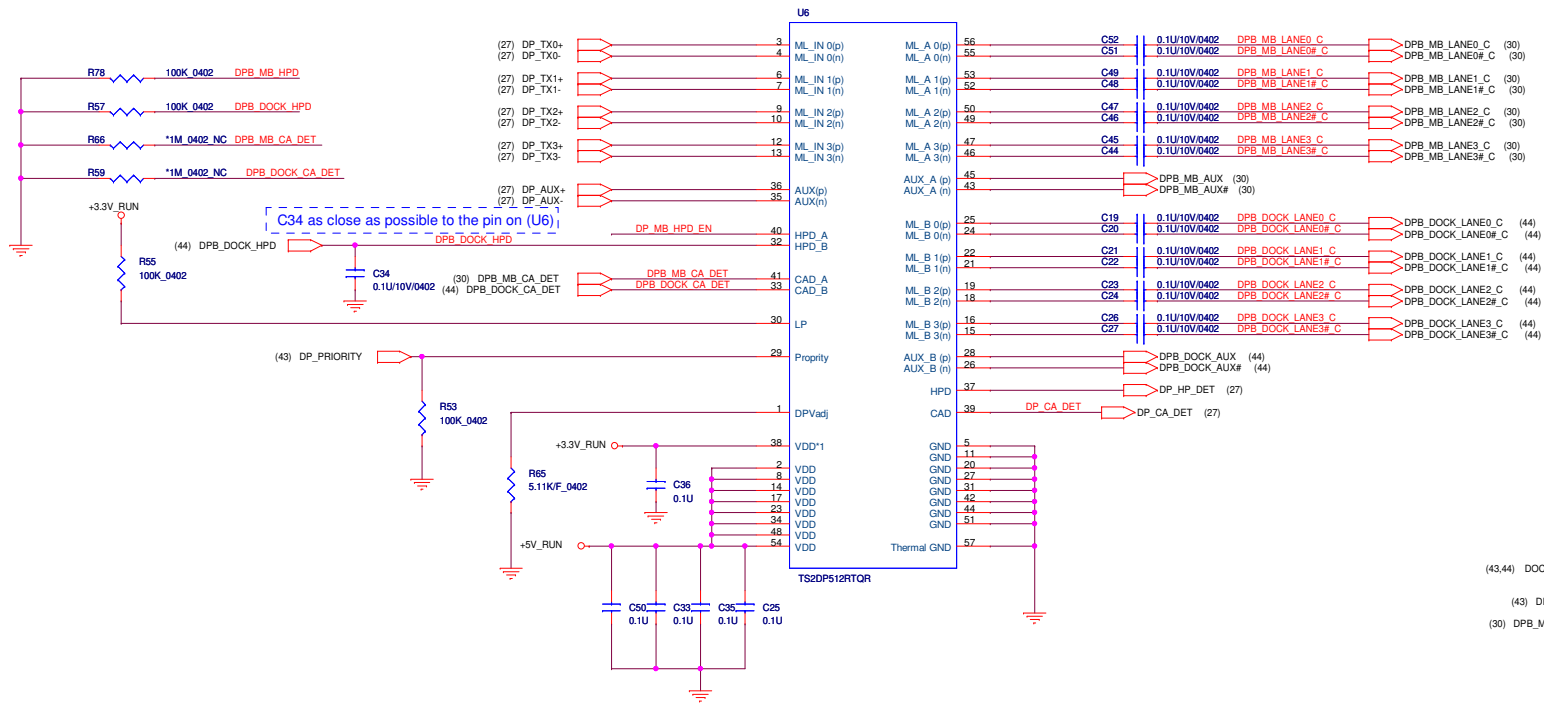
CHB_DIMM0_TOP Layer

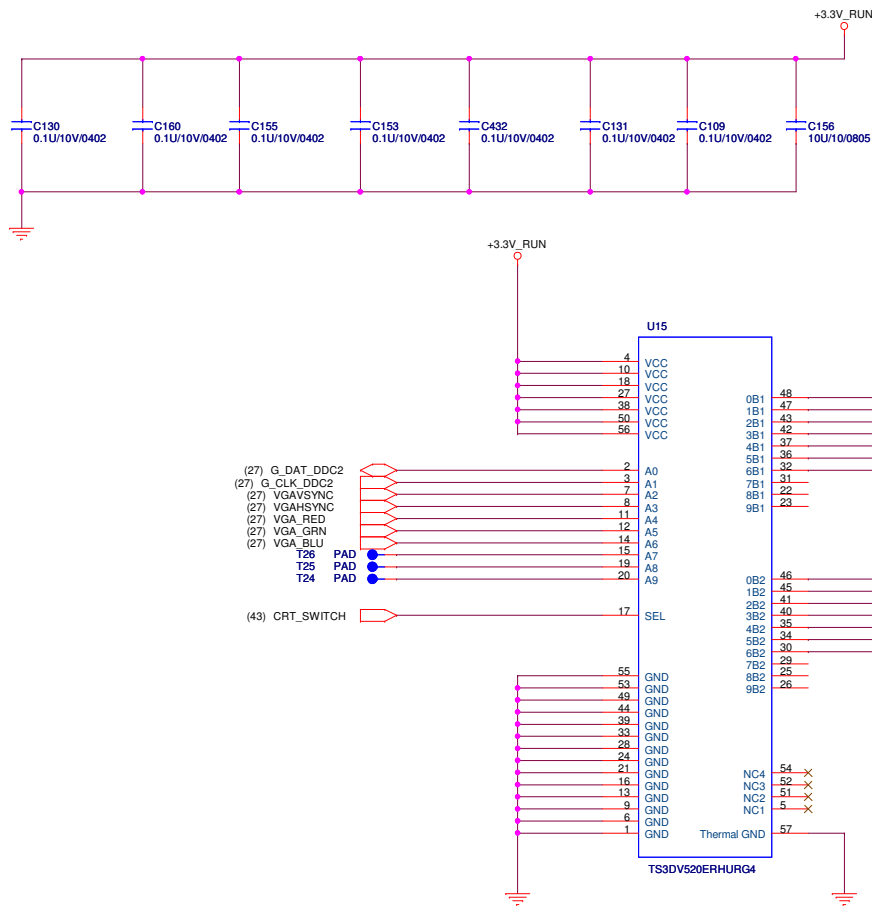


**Place these
caps close to
VTT1 and VTT2**

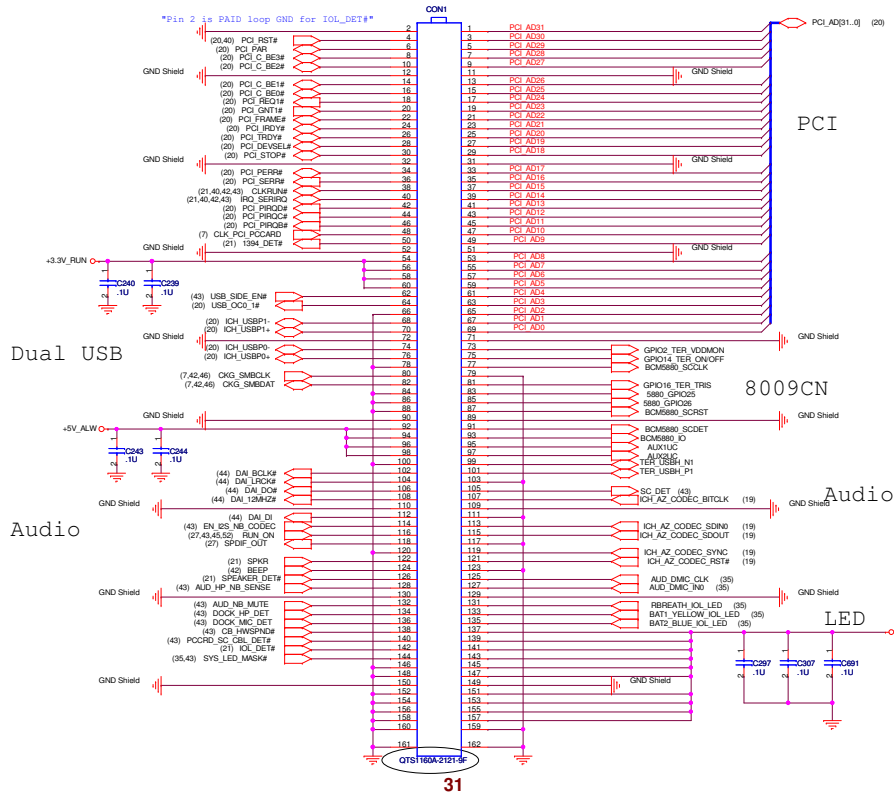


	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	

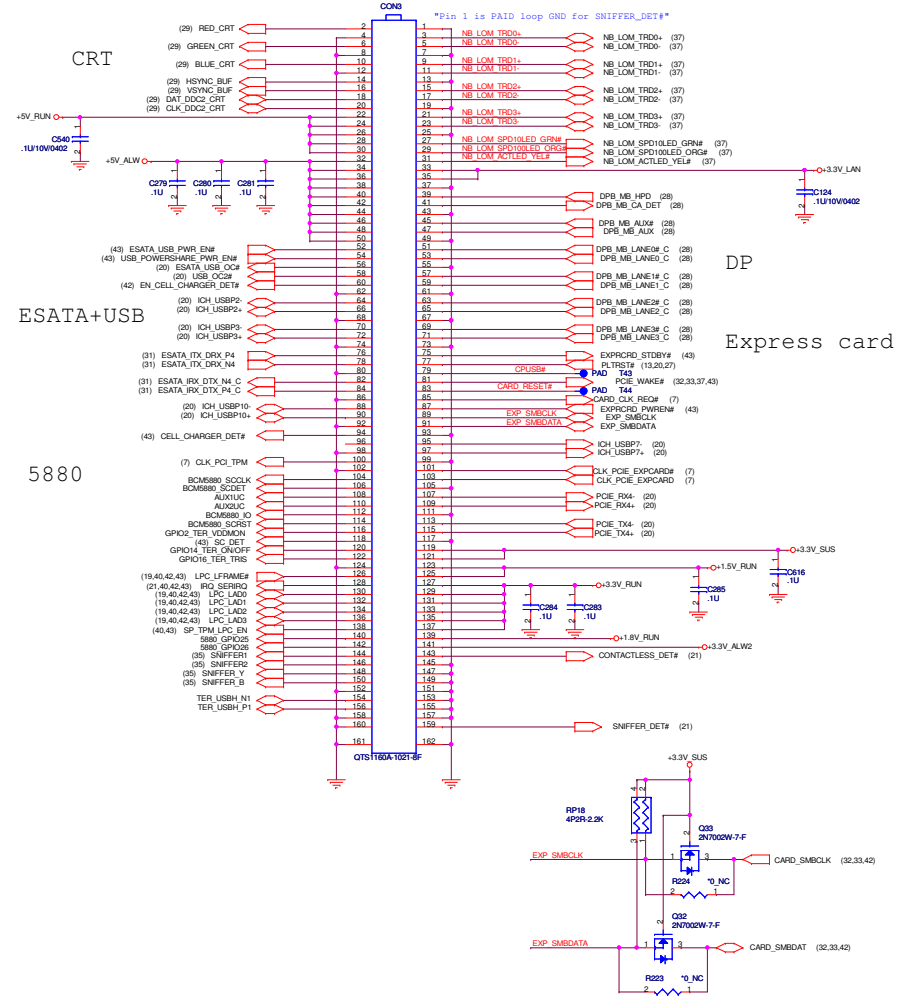




IOL CONNECTER



IOR CONNECTER



SATA1

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

GND1 RXP
RXN
GND2
TXN
TXP
GND3

3.3V_0
3.3V_1
3.3V_2
GND4
GND5
GND6
SV_0
SV_1
SV_2
GND7
RSVD
GND8
12V_0
12V_1
12V_2

SATA_TX+ (19)
SATA_TX+ (19)
SATA_RXN# C 0.01U/25V
SATA_RXP# C 0.01U/25V
SATA_RX+ (19)
SATA_RX# (19)

C651
0.1U_16V

+3.3V_HDD

HDD2_DET# (20)

+5V_HDD

+5V_HDD

C659
*0.1U/10V_NC

C680
*1000P/50V_NC

LD2522H-SA3L6

The schematic diagram illustrates the SATA interface for the L2122H-S0FL8. The interface is connected to the SATA_TX0+, SATA_TX-, SATA_RX0-, and SATA_RX0+ signals. The power supply connections are shown for 3.3V_HDD, 5V_HDD, and 5V_HDD. The diagram includes a table of component values and a list of component footprints.

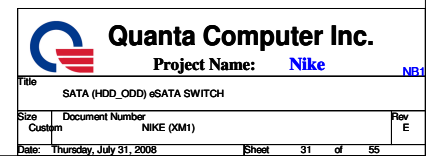
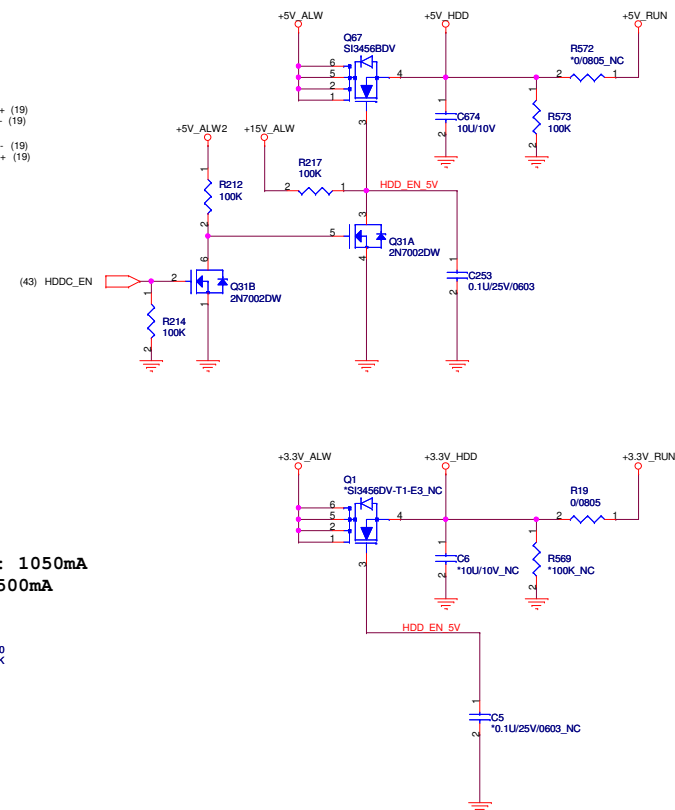
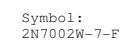
Component	Value	Footprint
C255	0.01u/25V	C255
C256	0.01u/25V	C256
C257	0.1u/16V	C257
C681	0.1u/10V_NC	C681
C670	*1000P/50V_NC	C670

Component footprints: C255, C256, C257, C681, C670.

684
U_10V_0805

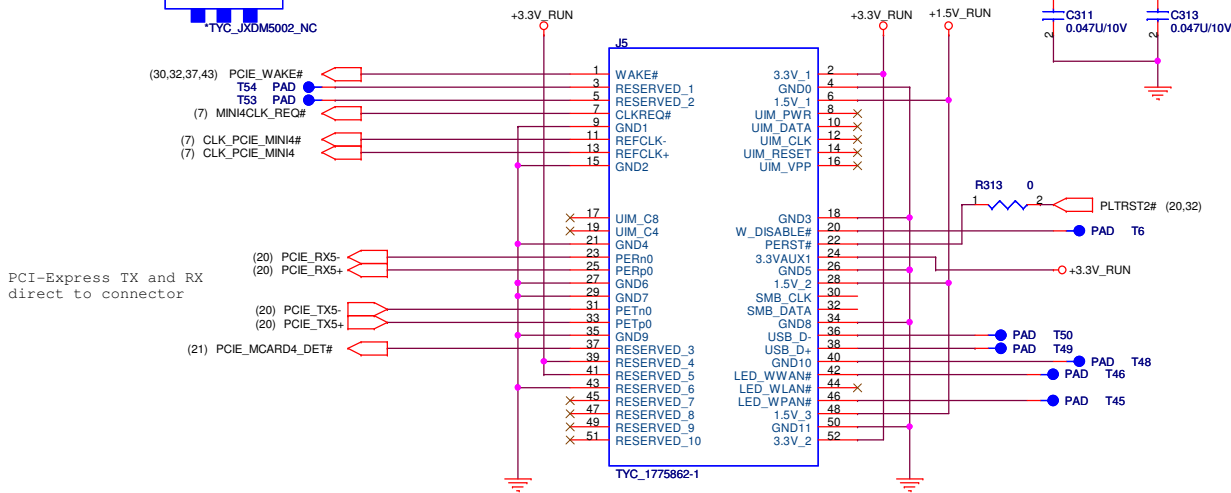
C686 0.1U_16V

C685 0.1U_16V

[illegible]



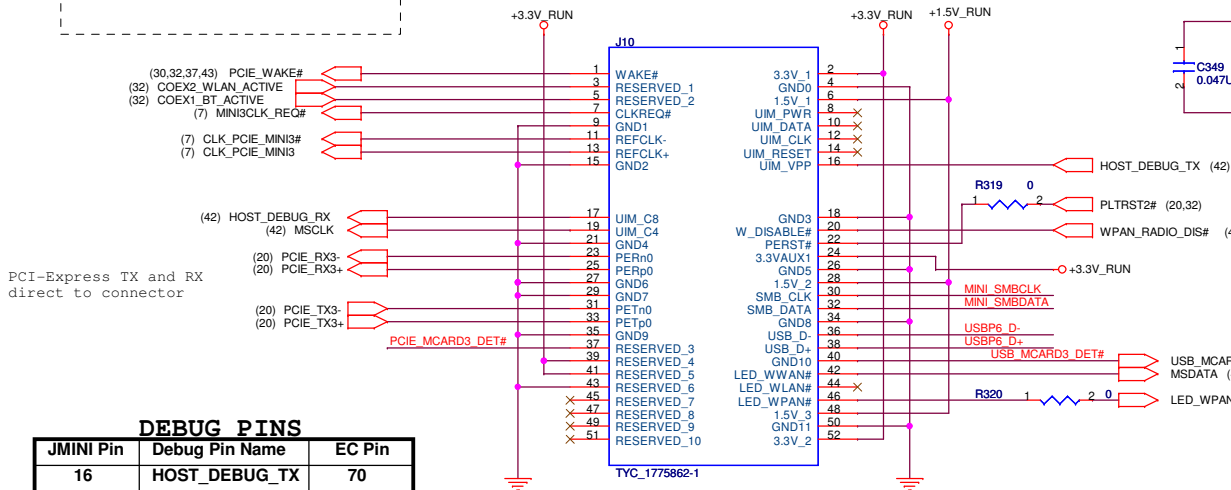
Robson connector



Footprint for XM1 Only

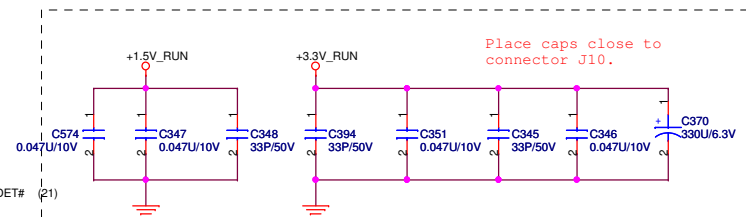
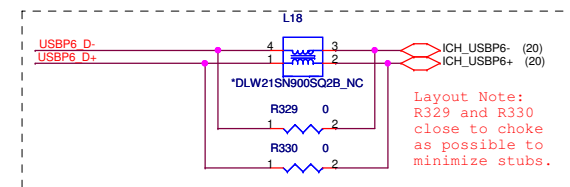
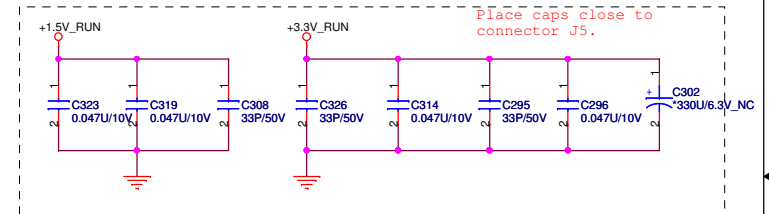
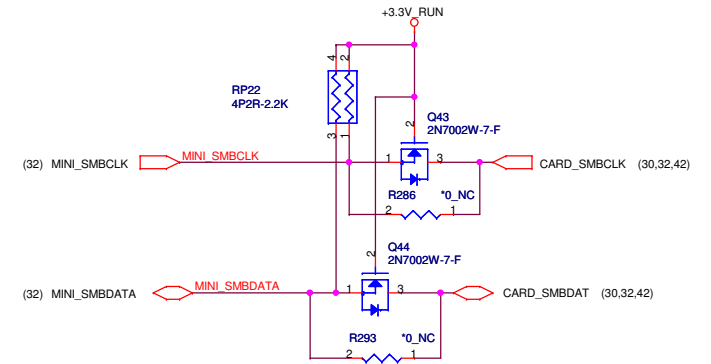


MiniCard UWB/BT connector



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

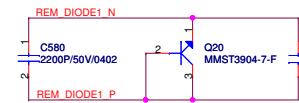


Quanta Computer Inc.
Project Name: **Nike**

Title: MINI CARD

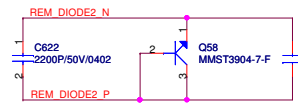
Size: Custom Document Number: NIKE (XM1) Rev: E

Date: Thursday, July 31, 2008 Sheet: 33 of 55



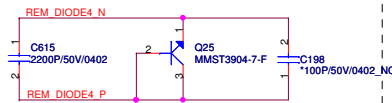
Put C580 close to Guardian.
Put C100 close to Diode

Place under CPU



Put C622 close to Guardian.
Put C453 close to Diode

Skin Temperature

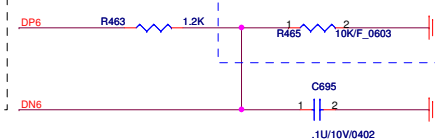


Put C615 close to Guardian.
Put C198 close to Diode

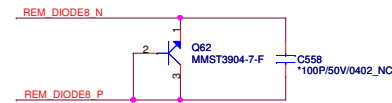
Place under DIMM Channel 1 (TOP)

R465 is a thermistor

Place R465 on BOT for Primary HDD (CN2)



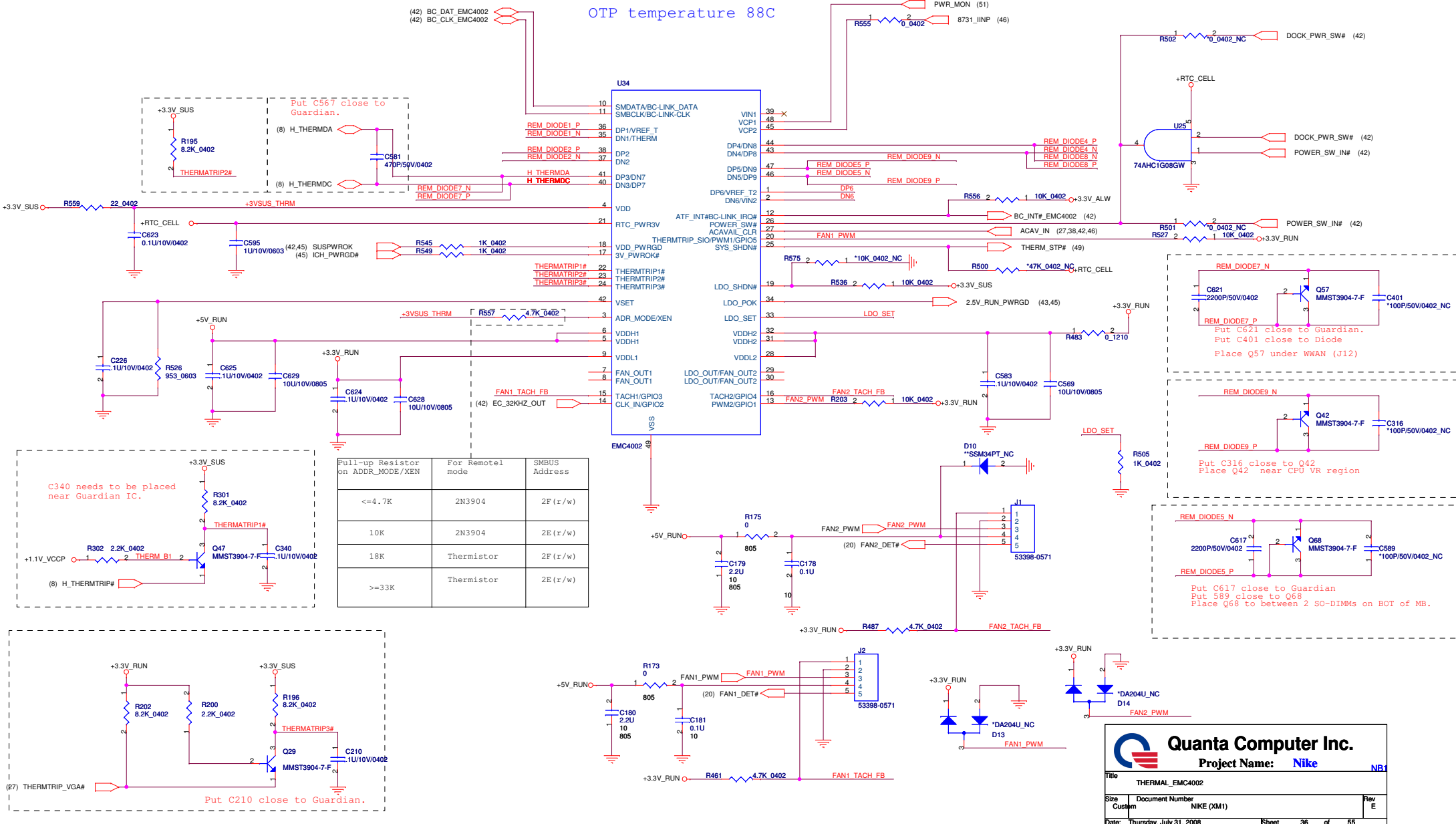
Put R463 and C589 close to Guardian.

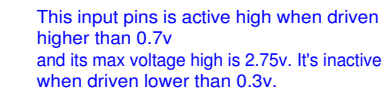


Put C558 close to Diode

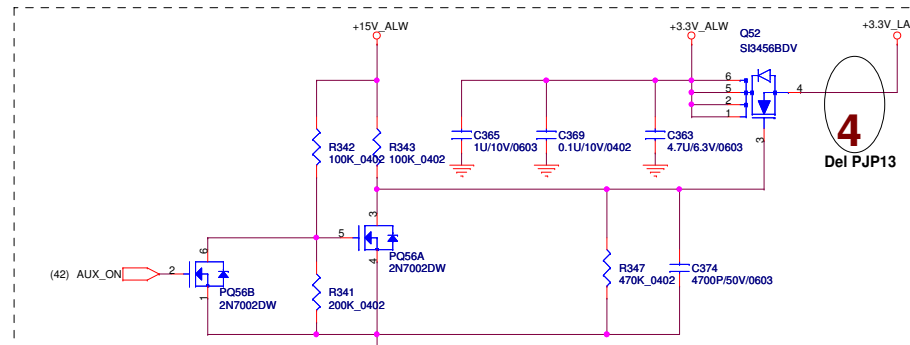
Place under DIMM Channel 2(TOP)

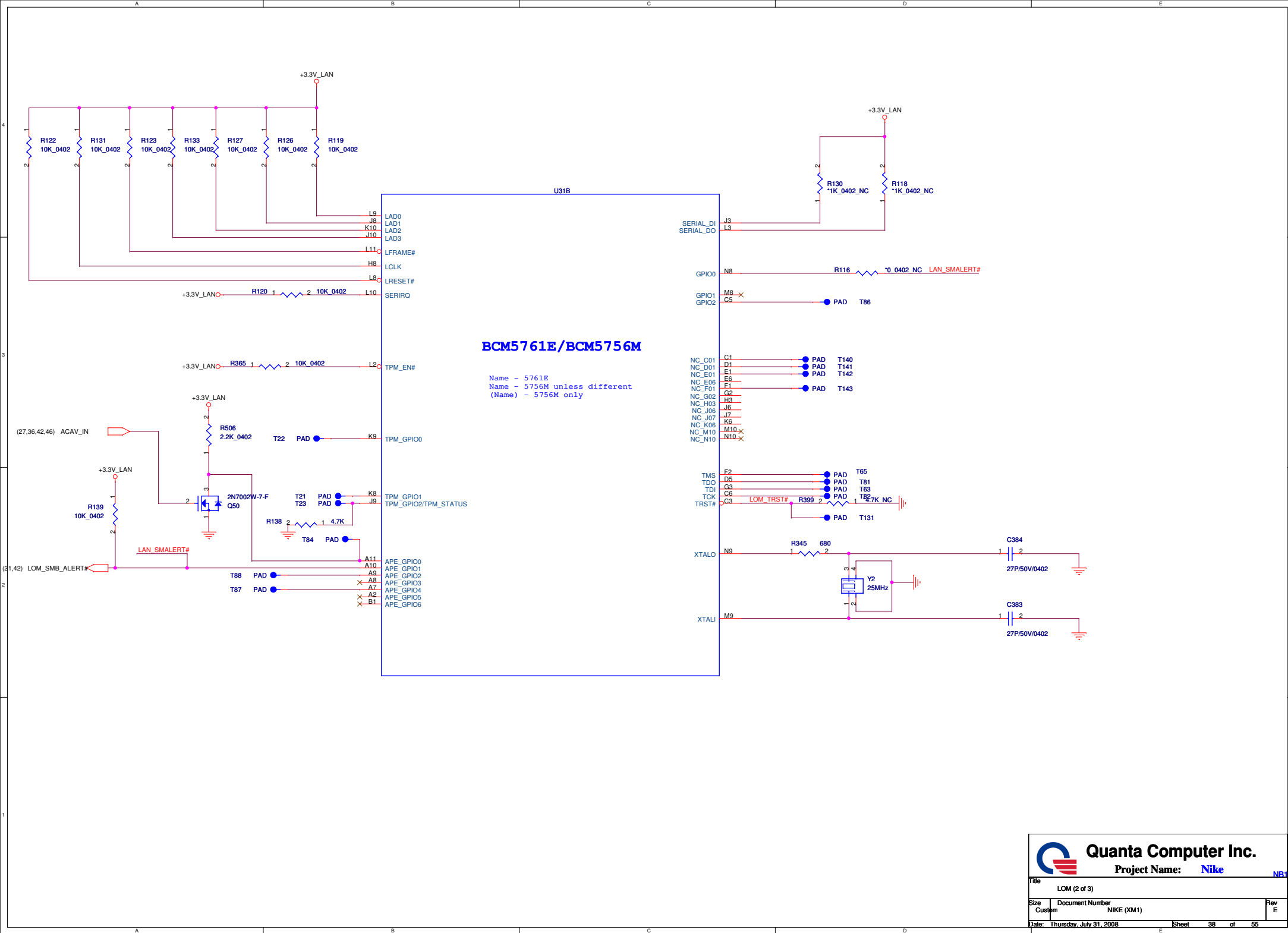
OTP temperature 88C

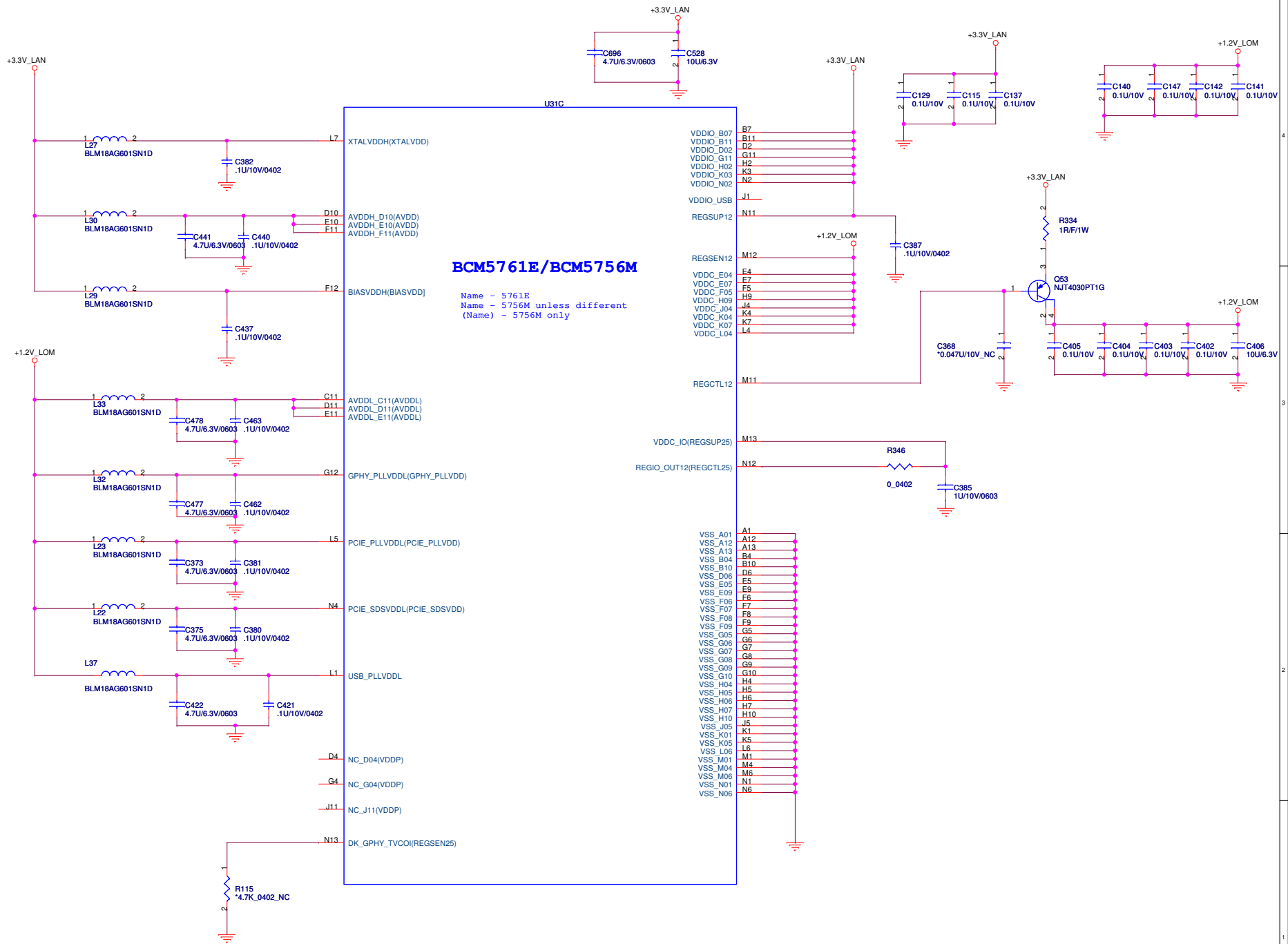




```
Name - 5761E
Name - 5756M unless different
(Name) - 5756M only
```







BCM5761E/BCM5756M

Name - 5761E
Name - 5756M unless different
(Name) - 5756M only

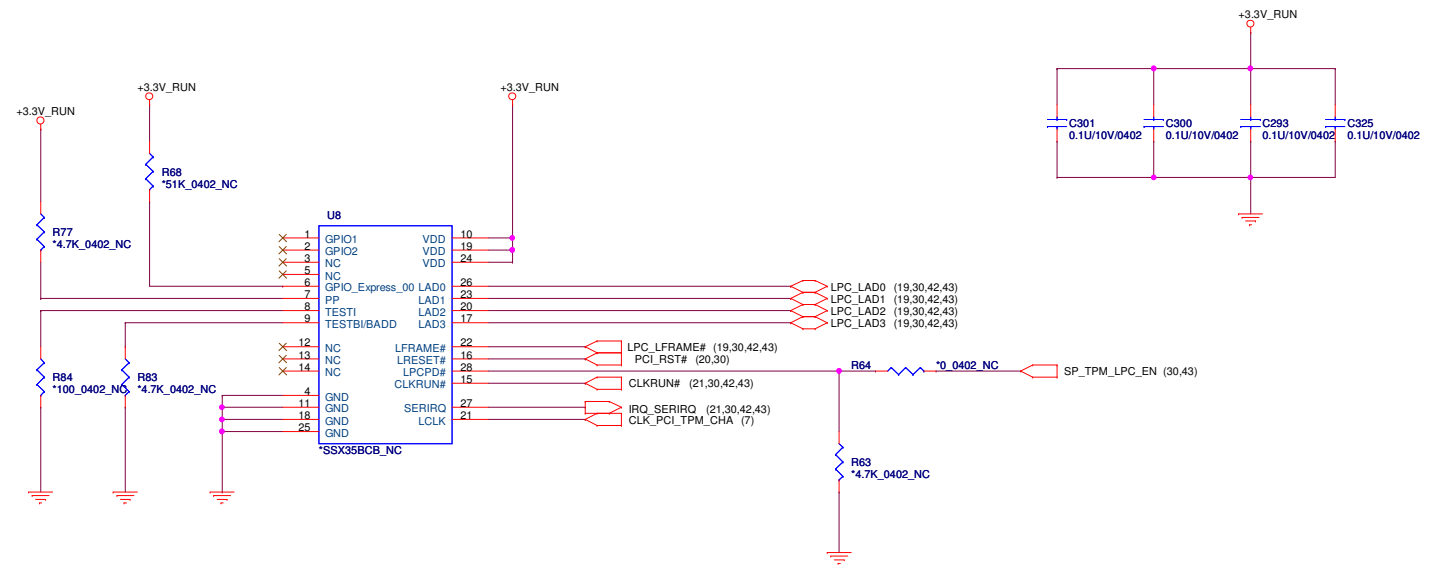
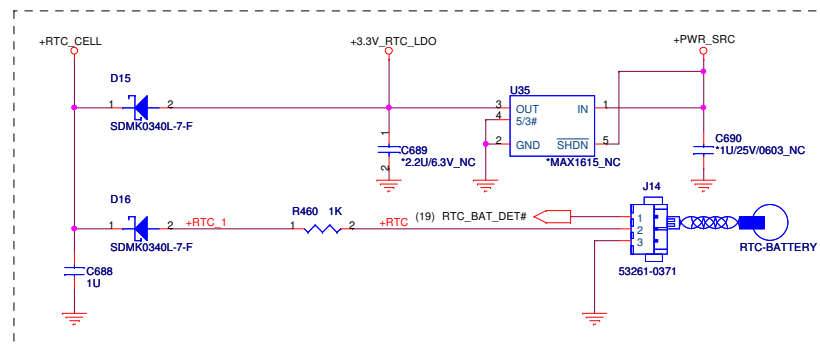
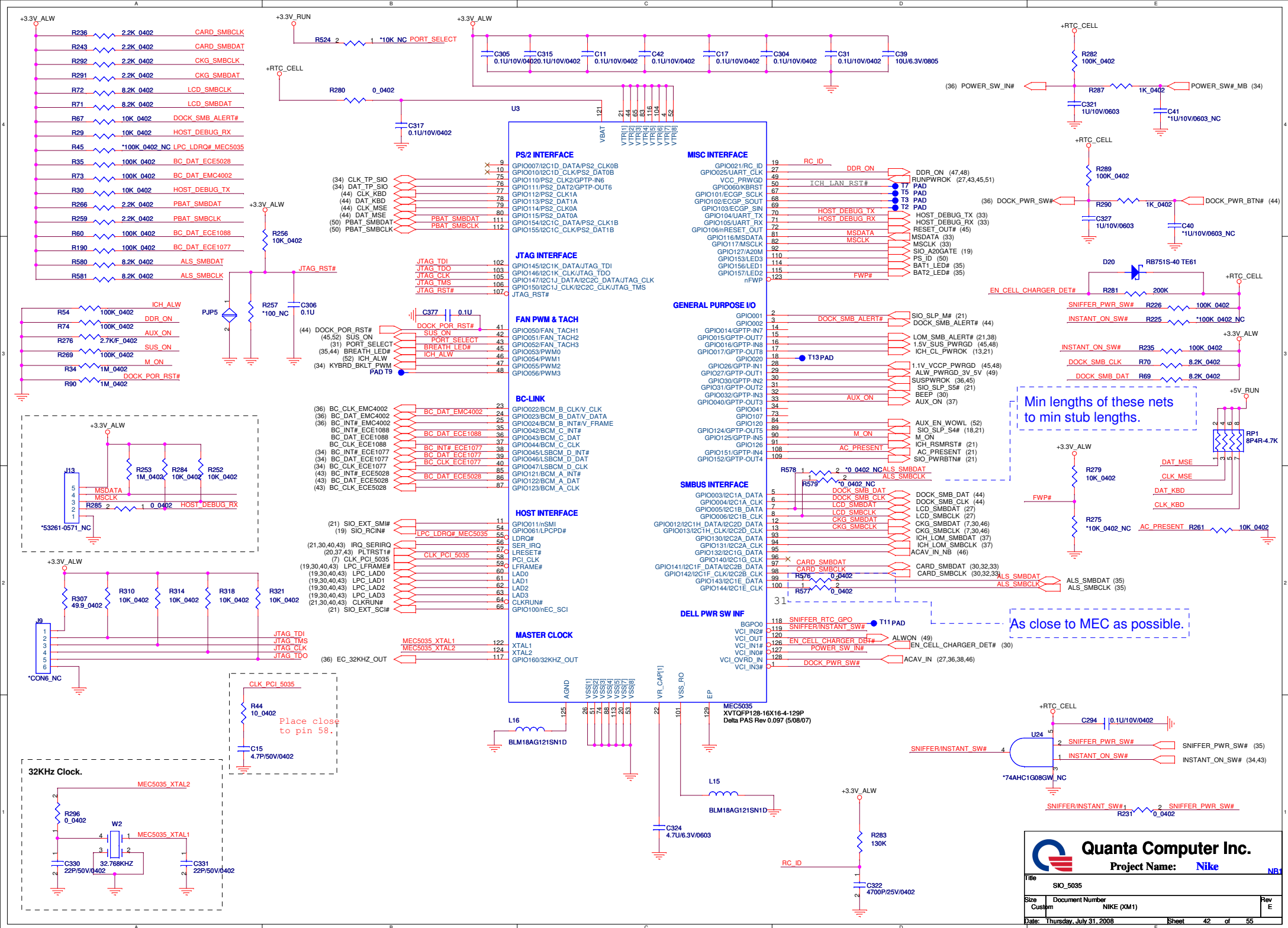


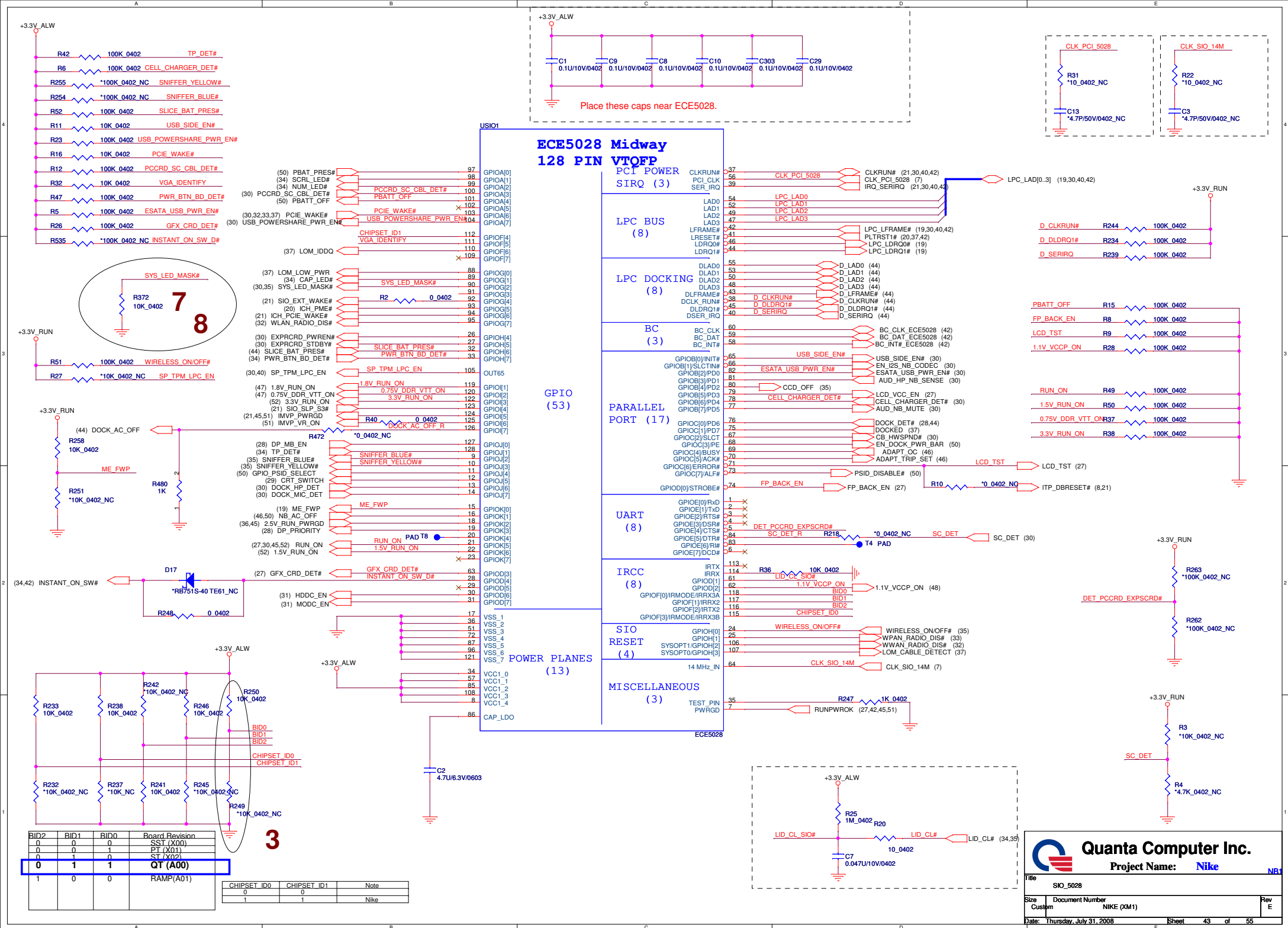
Table1

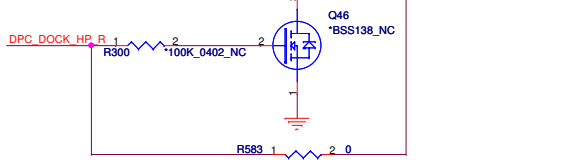
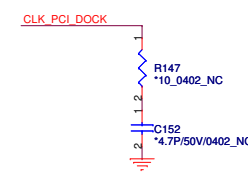
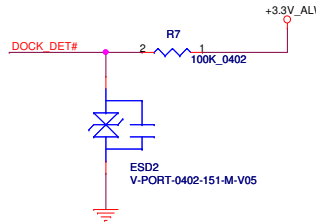
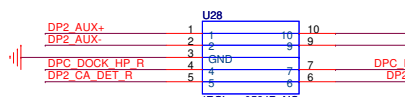
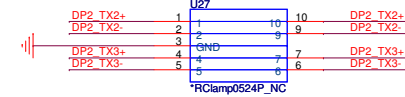
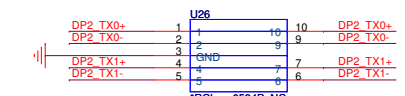
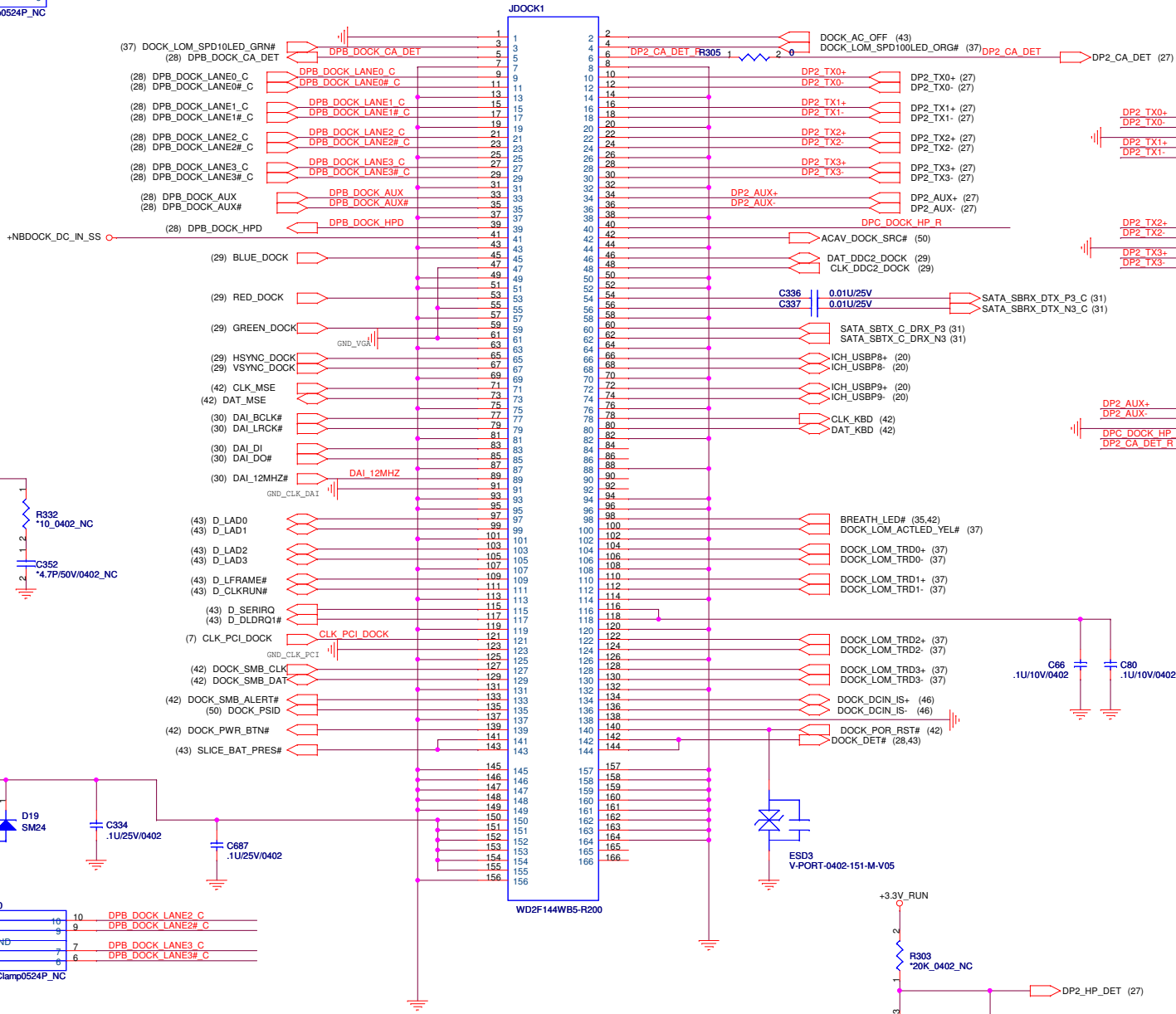
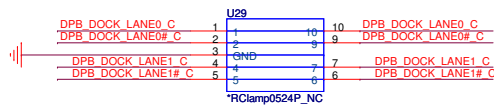
BOM option scheme for USH TPM vs China TPM				
		C0 USH	No TPM	
MB	MB, U8	NC	NC	
	MB, R27	NC	NC	
	MB, R63	NC	NC	
	MB, R64	NC	NC	
	R77, R68, R84, R83	NC	NC	
	MB, R149	POP	POP	
	MB, R151	NC	NC	
	MB, R156	NC	POP	
	MB, R434	POP	NC	

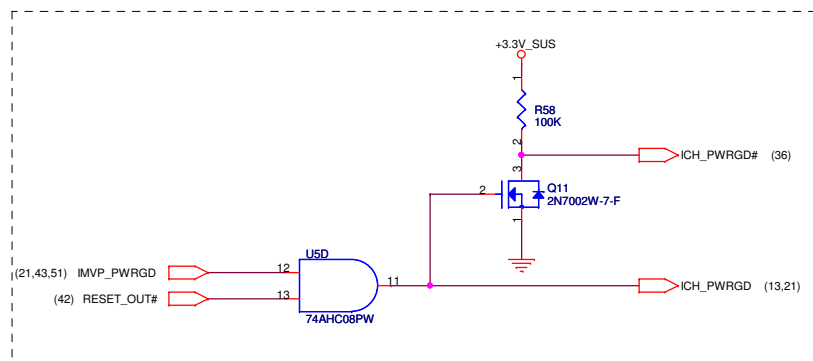
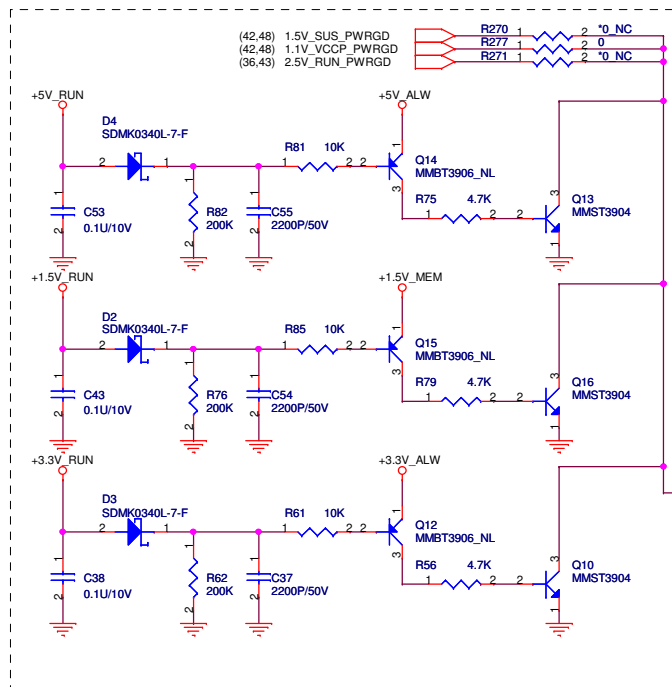
RTC BATTERY



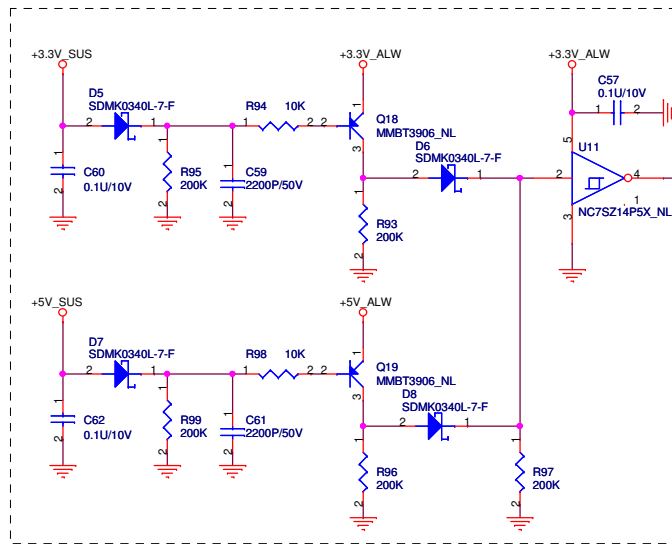
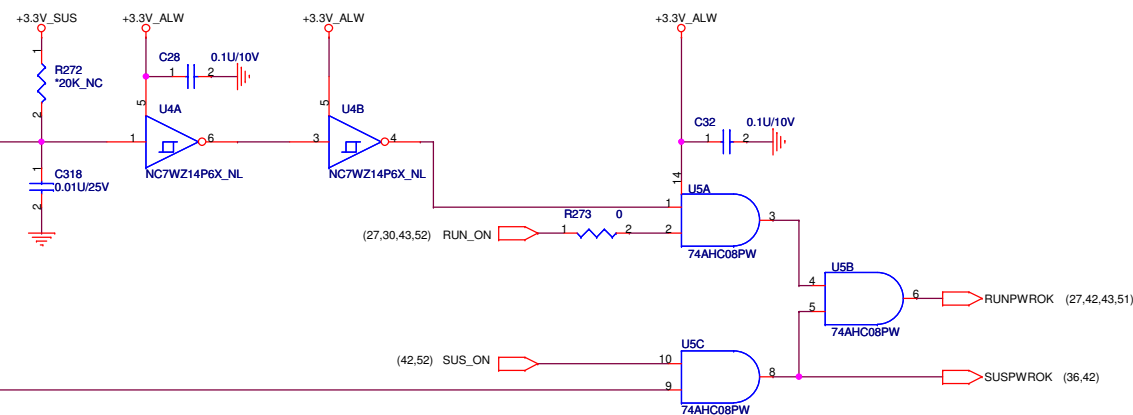


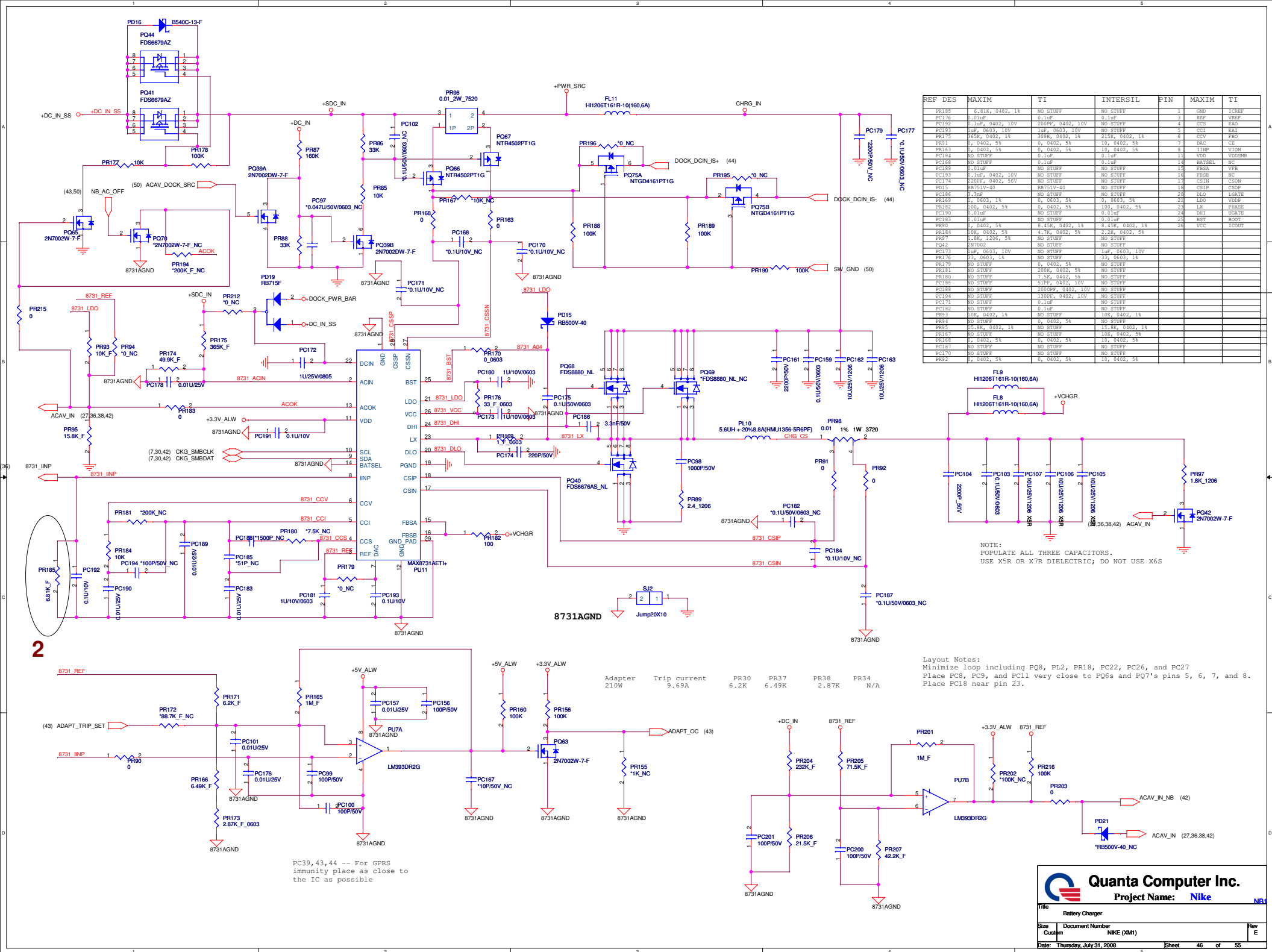






Keep Away from high speed buses

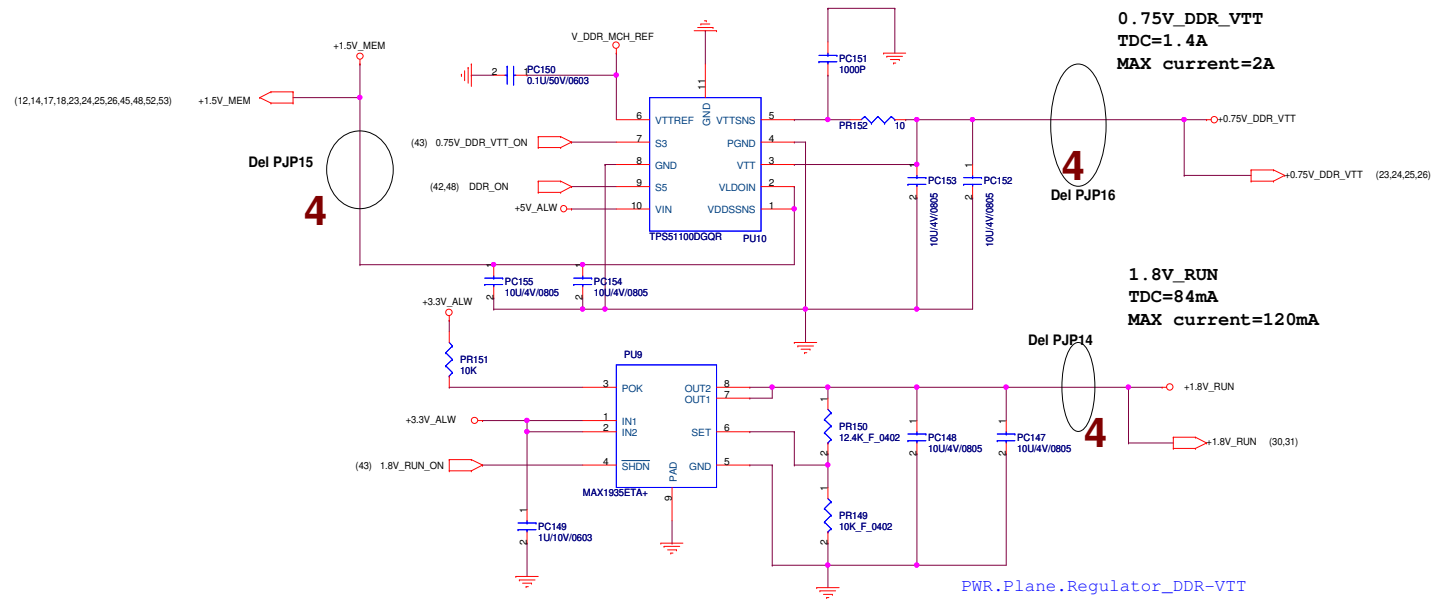




REF	DES	MAXIM	TI	INTERSIL	PIN	MAXIM	TI
PR185	6.81K, 0402, 1%	NO STUFF	NO STUFF	1	GND	ICREF	
PC176	0.1uF, 0402, 10V	0.1uF	0.1uF	3	REF	VREF	
PC193	1uF, 0603, 10V	200PF, 0402, 10V	NO STUFF	4	CCS	EAG	
PR175	15K, 0402, 1%	10K, 0402, 1%	215K, 0402, 1%	5	CC1	EAT	
PR191	0.0402, 5%	0.0402, 5%	10, 0402, 5%	6	CC2	CE	
PR163	0.0402, 5%	0.0402, 5%	10, 0402, 5%	8	11NP	V10M	
PC184	NO STUFF	0.1uF	0.1uF	11	VDD	VDDSRM	
PC189	NO STUFF	0.1uF	0.1uF	14	BATSEL	NC	
PC189	0.1uF	NO STUFF	NO STUFF	15	FBIA	VFB	
PC193	0.1uF, 0402, 10V	NO STUFF	NO STUFF	16	FBIB	NC	
PC174	220PF, 0402, 50V	NO STUFF	NO STUFF	17	CS1B	CSGN	
PC195	RB751V-40	RB751V-40	NO STUFF	18	CS1P	CSOP	
PC186	3.3K	NO STUFF	NO STUFF	20	DLO	LGATE	
PR189	0.0603, 1%	0.0603, 5%	0.0603, 5%	21	UD0	VDSR	
PR182	100, 0402, 5%	0.0402, 5%	100, 0402, 5%	23	LX	PHASE	
PC190	0.01uF	NO STUFF	0.01uF	24	DRI	UGATE	
PC183	0.01uF	NO STUFF	0.01uF	25	BS1	BOOT	
PR190	0.0402, 5%	8.45K, 0402, 1%	8.45K, 0402, 1%	26	CC2	ICOUT	
PR184	10K, 0402, 5%	4.7K, 0402, 5%	2.2K, 0402, 5%	27	CC2	ICOUT	
PR191	0.0402, 5%	NO STUFF	NO STUFF	28	CC2	ICOUT	
PC173	1uF, 0603, 10V	NO STUFF	1uF, 0603, 10V	29	CC2	ICOUT	
PR179	NO STUFF	0.0402, 5%	NO STUFF	30	CC2	ICOUT	
PR181	NO STUFF	200K, 0402, 5%	NO STUFF	31	CC2	ICOUT	
PR180	NO STUFF	7.5K, 0402, 5%	NO STUFF	32	CC2	ICOUT	
PC185	NO STUFF	100K, 0402, 10V	NO STUFF	33	CC2	ICOUT	
PC188	NO STUFF	200PF, 0402, 10V	NO STUFF	34	CC2	ICOUT	
PC194	NO STUFF	100PF, 0402, 10V	NO STUFF	35	CC2	ICOUT	
PC171	NO STUFF	0.1uF	NO STUFF	36	CC2	ICOUT	
PC182	NO STUFF	0.1uF	NO STUFF	37	CC2	ICOUT	
PR183	10K, 0402, 1%	NO STUFF	10K, 0402, 1%	38	CC2	ICOUT	
PR194	NO STUFF	0.0402, 5%	NO STUFF	39	CC2	ICOUT	
PR195	15.8K, 0402, 1%	NO STUFF	15.8K, 0402, 1%	40	CC2	ICOUT	
PR188	0.0402, 5%	NO STUFF	NO STUFF	41	CC2	ICOUT	
PC187	NO STUFF	NO STUFF	NO STUFF	42	CC2	ICOUT	
PC170	NO STUFF	NO STUFF	NO STUFF	43	CC2	ICOUT	
PR192	0.0402, 5%	NO STUFF	NO STUFF	44	CC2	ICOUT	


NOTE:
POPULATE ALL THREE CAPACITORS.
USE X5R OR X7R DIELECTRIC; DO NOT USE X6S

Layout Notes:
Minimize loop including PQ8, PL2, PR18, PC22, PC26, and PC27
Place PC8, PC9, and PC11 very close to PQ6 and PQ7's pins 5, 6, 7, and 8.
Place PC18 near pin 23.

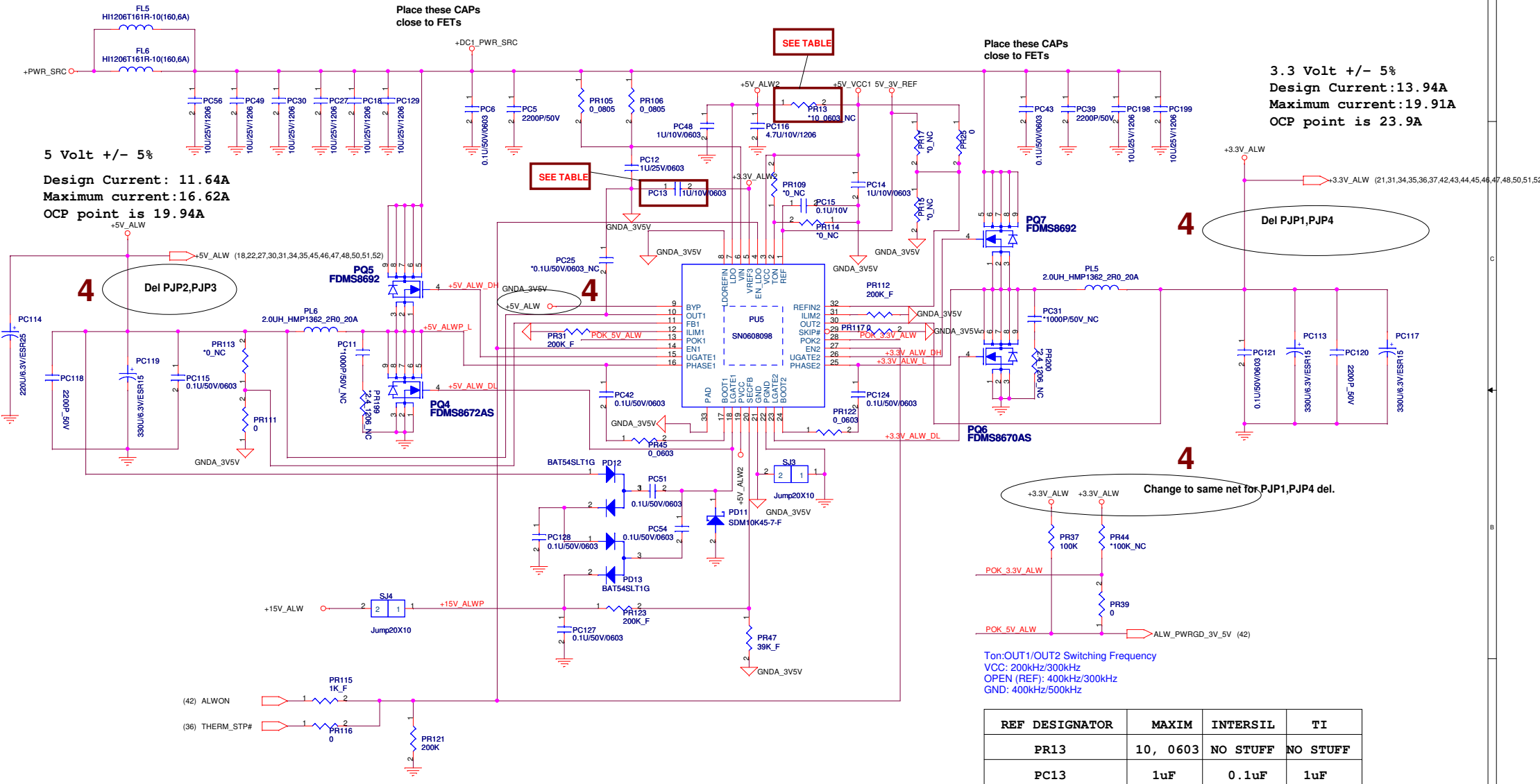


M'09



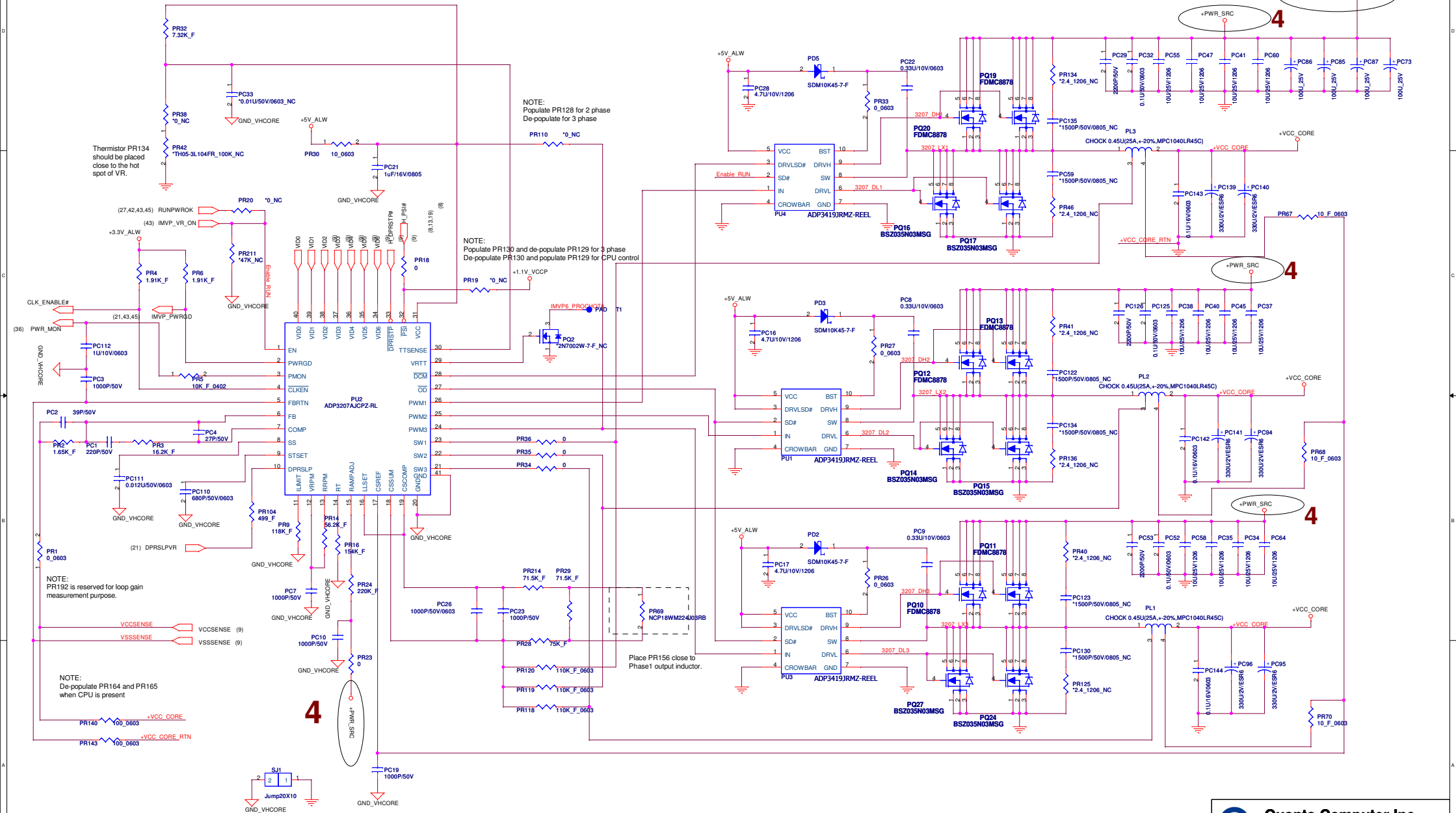
 Quanta Computer Inc.		Project Name: Nike		NBT
Title: 1.1V_VCCP and 1.5V_MEM				
Size Custom	Document Number NIKE (XM1)			Rev E
Date: Thursday, July 31, 2008		Sheet 48 of 55		

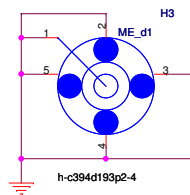
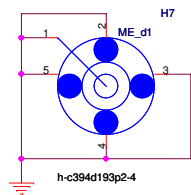
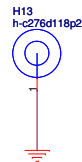
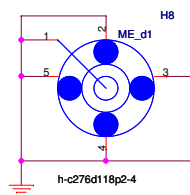
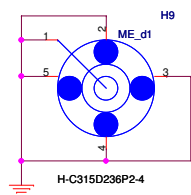
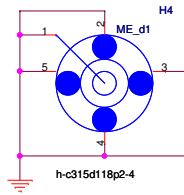
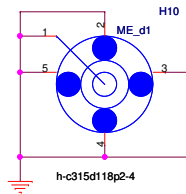
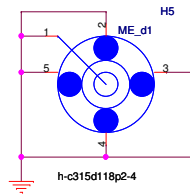
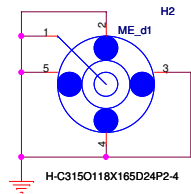
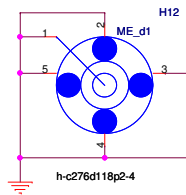
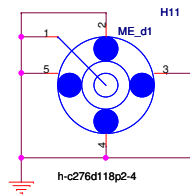
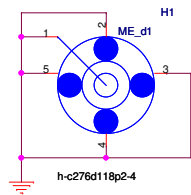
M'09
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+3.3V_ALW2/+15V_ALW



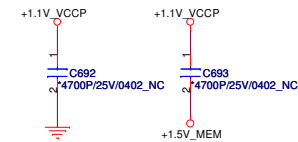
IMVP-6 solution for
Penryn:
Iccmax: 47A
OCP: 56A, Intel spec: 50A

del PJP6,PJP8





Stitching caps



EMI Clips

